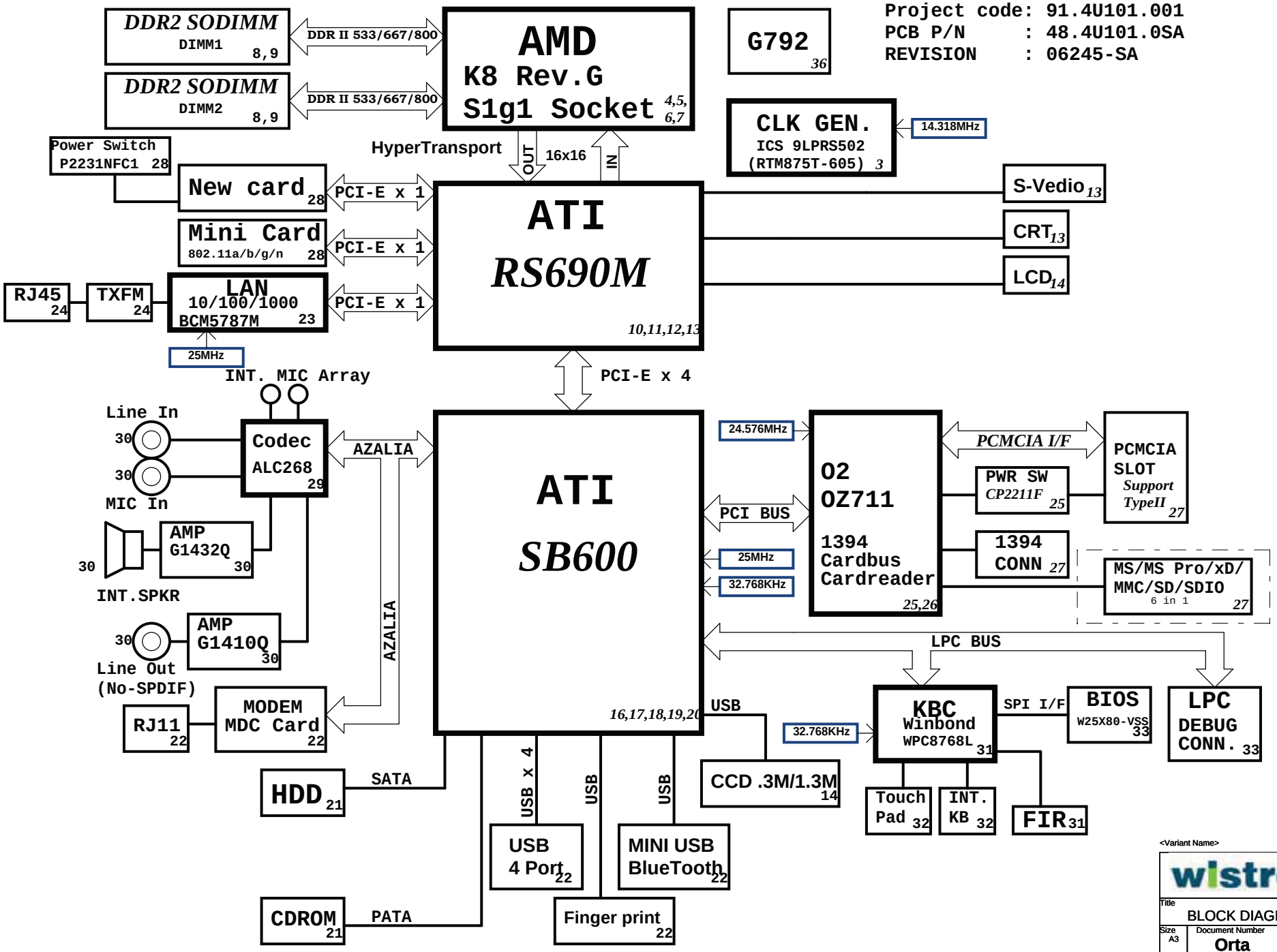
Orta Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 1 of 46

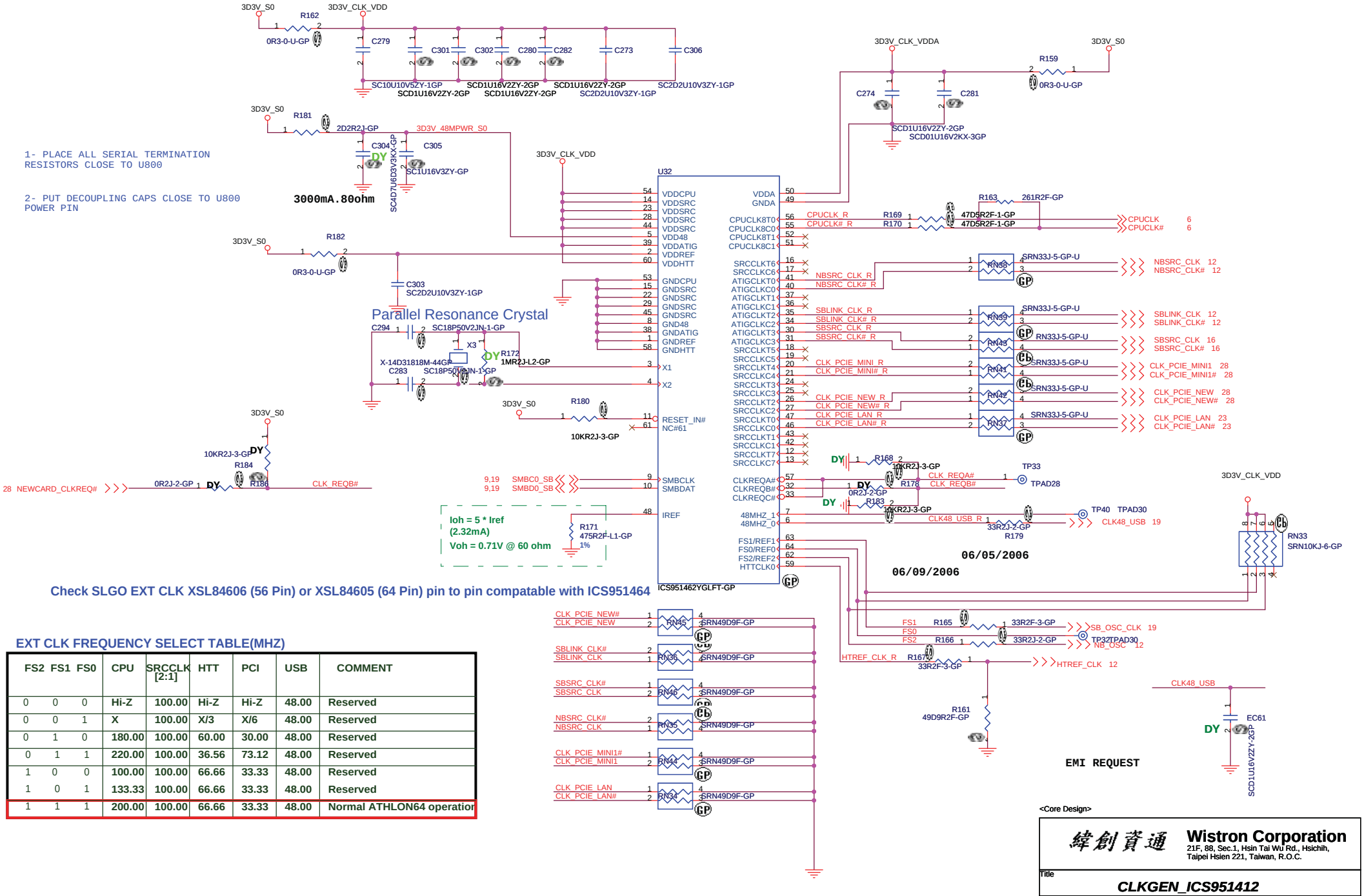
SA: 07/31/06 Start

SB change
power team
1.change L7, L9 to 68.1R510.10D
2.changge U12 to 84.04706.037
3.change R66 to 10K ohm

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANGE HISTORY
Size: A3 | Document Number: Orta | Rev: SA
Date: Tuesday, December 12, 2006 | Sheet 2 of 46



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

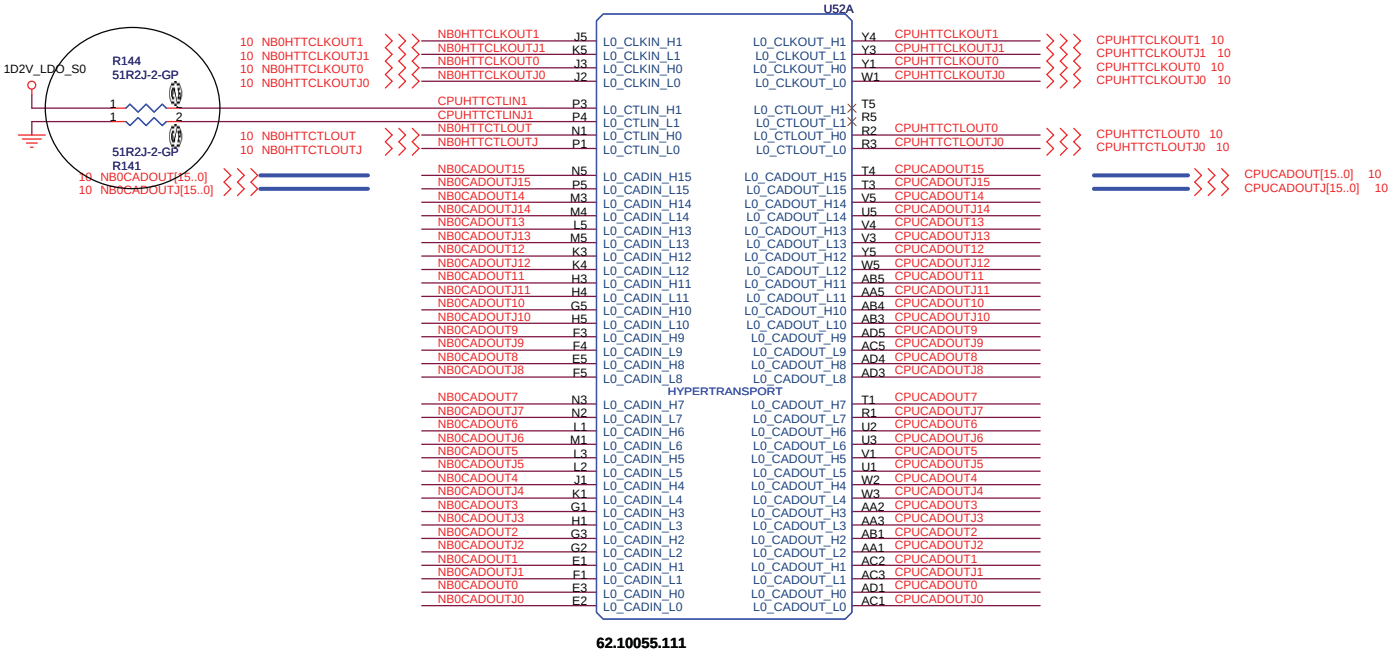
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS951412

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 3 of 46



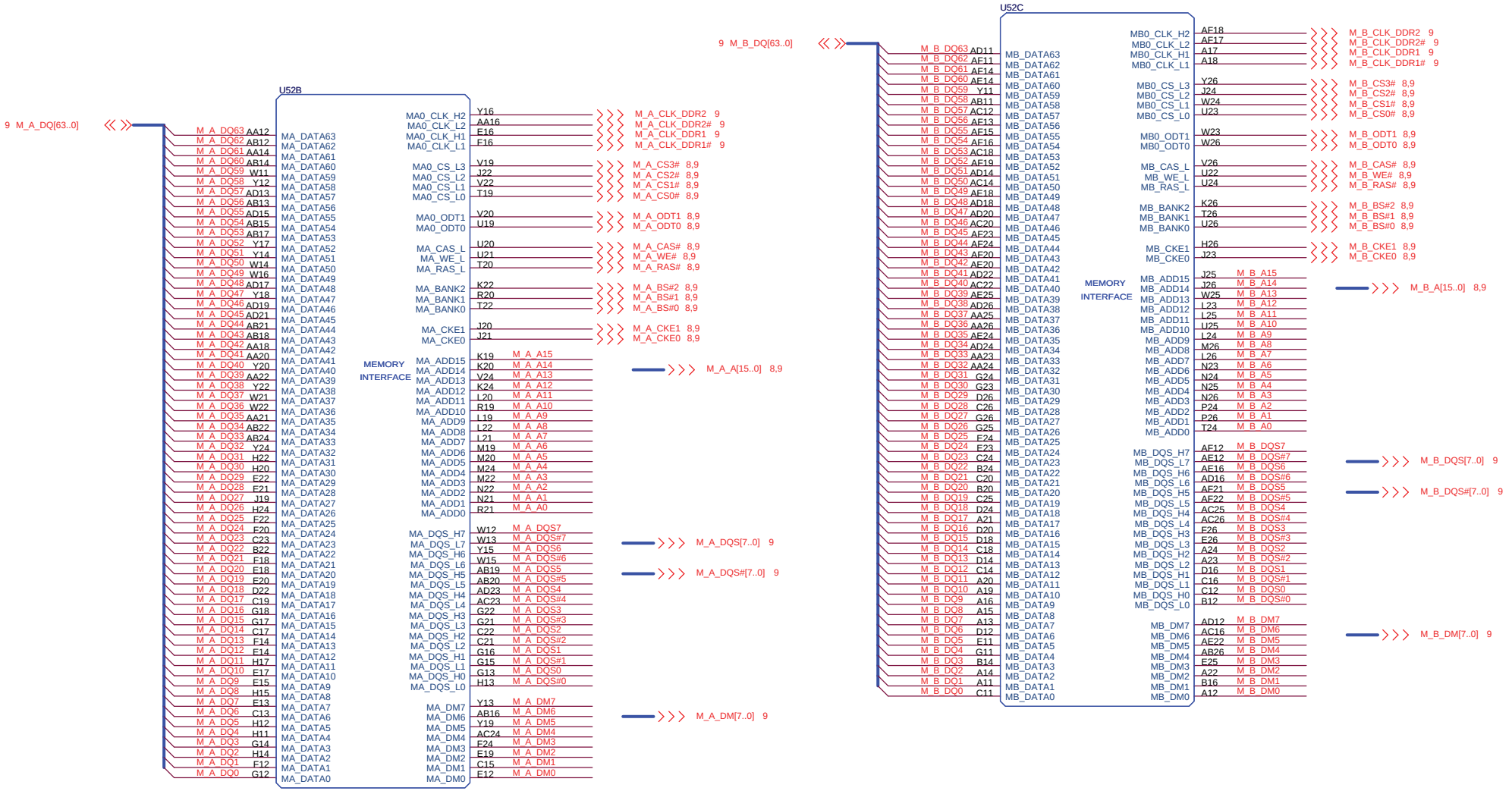
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(1/4)_HyperTransport I/F

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 4 of 46



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(2/4)_DDR**

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 5 of 46

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

Near To CPU

20061031 for Power Test

Remove these resistor when using EVT CPU

Change;Add

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

VREF_DDR_CLAW

LAYOUT: Locate close to CPU.

HDT Connectors

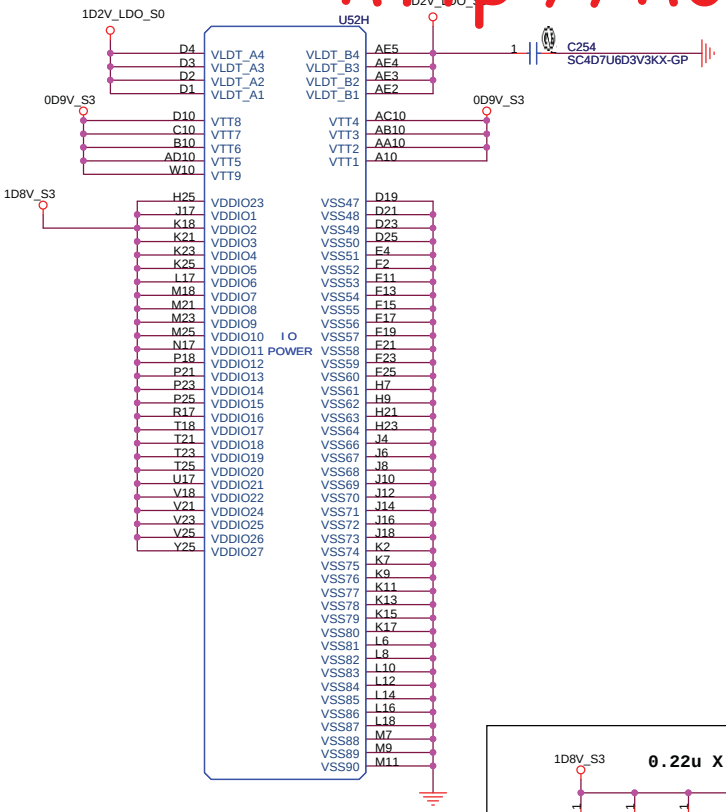
<Core Design>

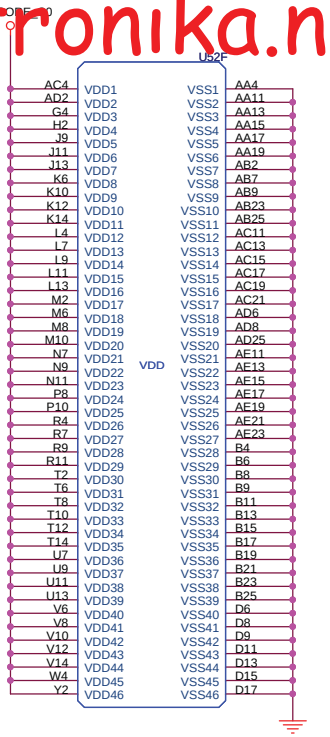
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

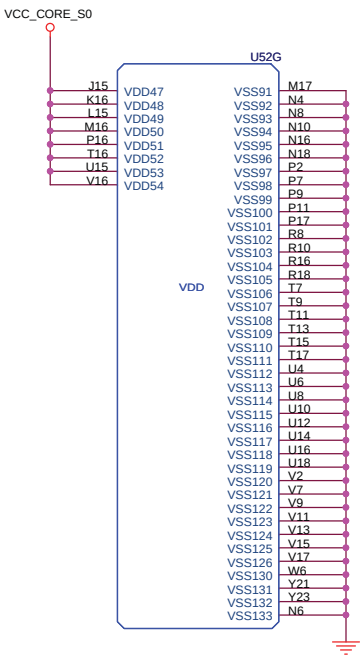
Title: CPU(3/4)_Control & Debug

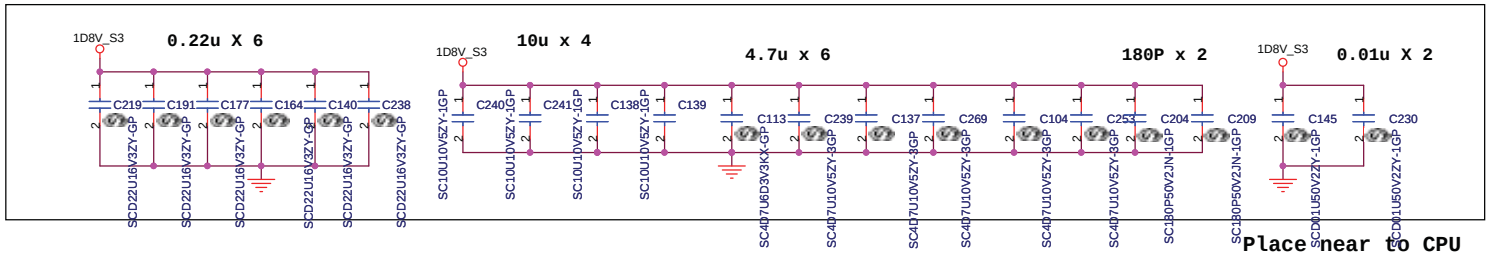
Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 6 of 46



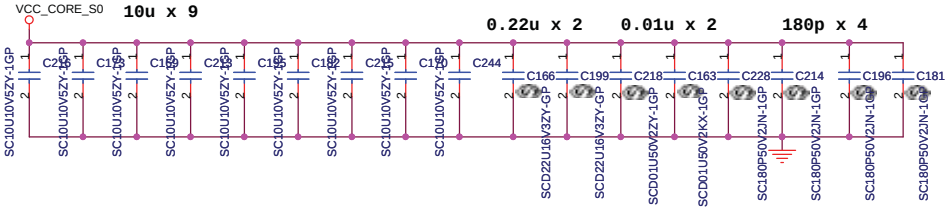


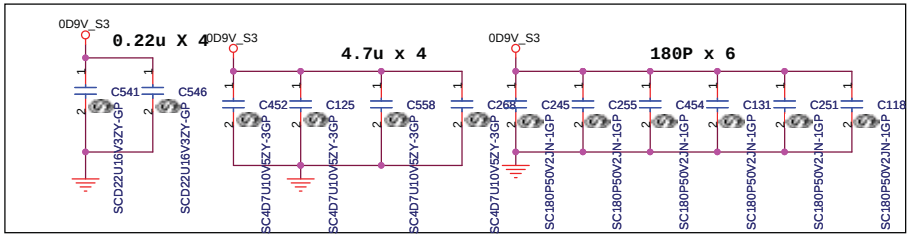


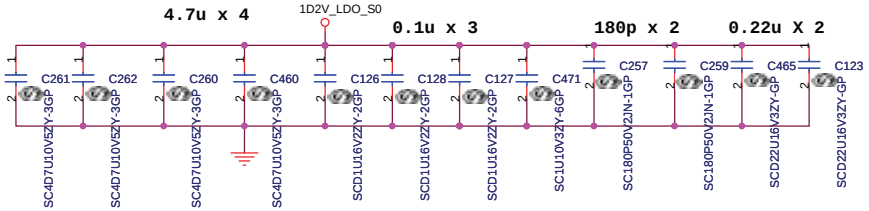


LAYOUT: Place on backside of processor.

Place near to CPU







<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU(4/4)_Power***

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 7 of 46

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

0D9V_S3

RN55 SRN47J-4GP: M_A_A2, M_A_A4, M_A_A6, M_A_A7
RN24 SRN47J-4GP: M_A_A10, M_A_BS#0, M_A_A1 — M_A_BS#0 5,9
RN30 SRN47J-4GP: M_A_WE# — M_A_WE# 5,9, M_A_ODT1 5,9
RN28 SRN47J-4GP: M_A_CS1#, M_A_CAS# — M_A_CS1# 5,9, M_A_CAS# 5,9
RN16 SRN47J-4GP — M_B_BS#2 5,9, M_B_CKE0 5,9
RN27 SRN47J-4GP: M_B_CS1# 5,9, M_B_WE# 5,9, M_B_CAS# 5,9, M_B_BS#0 5,9
RN18 SRN47J-4GP: M_B_A12, M_B_A9, M_B_A8 — M_B_CS2# 5,9
RN23 SRN47J-4GP: M_B_A10, M_B_A1, M_B_A3, M_B_A5
RN57 SRN47J-4GP — M_A_CS3# 5,9, M_A_A13 5,9, M_A_ODT0 5,9
RN56 SRN47J-4GP — M_A_CS0# 5,9, M_A_RAS# 5,9, M_A_BS#1 5,9, M_A_A0 5,9
RN19 SRN47J-4GP: M_A_A5, M_A_A3, M_A_A9, M_A_A8
RN21 SRN47J-4GP: M_B_A7, M_B_A6, M_B_A4, M_B_A2
RN25 SRN47J-4GP: M_B_A0 — M_B_RAS# 5,9, M_B_BS#1 5,9, M_B_CS0# 5,9
RN17 SRN47J-4GP: M_B_A15, M_B_A14, M_B_A11 — M_B_CKE1 5,9

0D9V_S3

RN15 SRN47J-4GP: M_A_BS#2, M_A_A12, M_A_CS2#, M_A_CKE0 — M_A_BS#2 5,9, M_A_CS2# 5,9, M_A_CKE0 5,9
RN54 SRN47J-4GP: M_A_A11, M_A_A14, M_A_A15, M_A_CKE1 — M_A_CKE1 5,9
RN29 SRN47J-4GP: M_B_A13 — M_B_ODT0 5,9, M_B_CS3# 5,9, M_B_ODT1 5,9

M_A_A[15..0] 5,9
M_B_A[15..0] 5,9

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

0D9V_S3

C526 C498 C235 C134 C207 C152 C184 C158 C502 C523 C194 C508 — SCD1U16V2ZY-2GP
C511 C141 C226 C171 — SC1000P50V3JN-GP
C500 C234 C208 C243 — SC10P50V2JN-4GP (C234, C208: DY; C243: DY)

Place these Caps near DM1

1D8V_S3

C518 C499 C510 C236 C161 — SC2D2U6D3V3KX-GP
C505 C512 C188 — SCD1U16V2ZY-2GP

Place these Caps near DM2

1D8V_S3

C135 C168 C178 C520 C192 — SC2D2U6D3V3KX-GP
C175 C147 C222 C201 — SCD01U50V2KX-1GP, SC180P50V2JN1GP

Cross Moat Cap

1D8V_S3

C211 C521 C515 — SC680P50V2KX-2GP

Place these Caps near PARALLEL TERMINATION

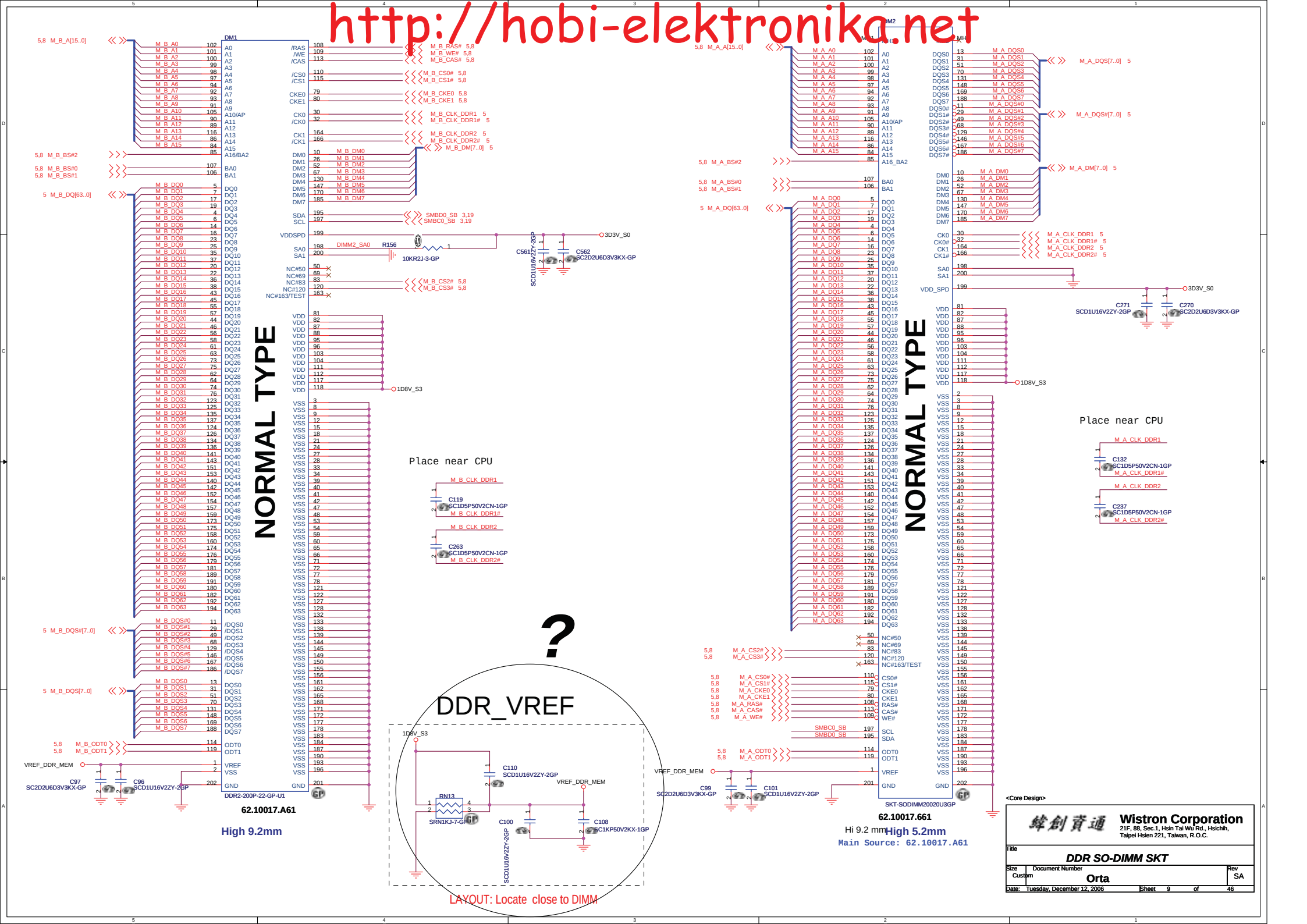
0D9V_S3 1D8V_S3

C524 C176 C189 C522 C136 C202 C142 C210 C167 C162 — SCD1U16V2ZY-2GP
C516 C187 C223 C519 C197 C190 C203 C217 — SCD1U16V2ZY-2GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DAMPING & TERMINATION
Size: A3 | Document Number: Orta | Rev: SA
Date: Tuesday, December 12, 2006 | Sheet 8 of 46

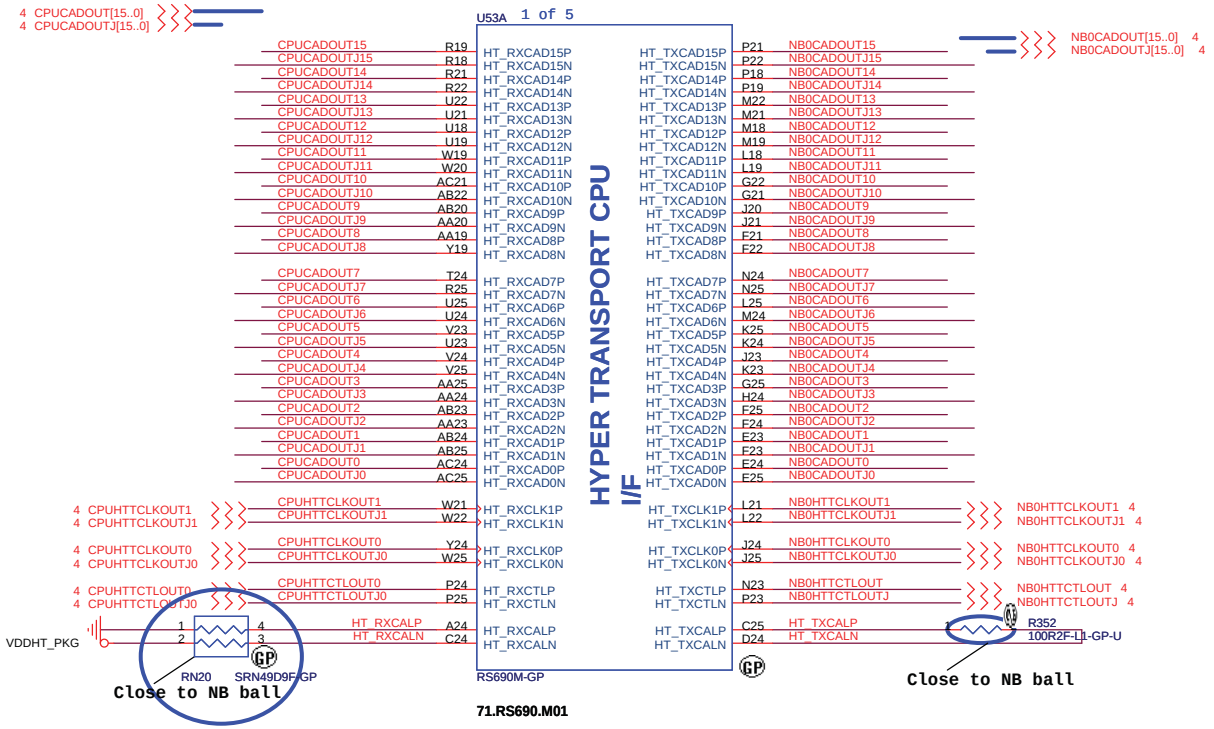


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR SO-DIMM SKT
Size: Custom
Document Number: Orta
Rev: SA
Date: Tuesday, December 12, 2006
Sheet 9 of 46

CLAW HAMMER TO NB

NB TO CLAW HAMMER



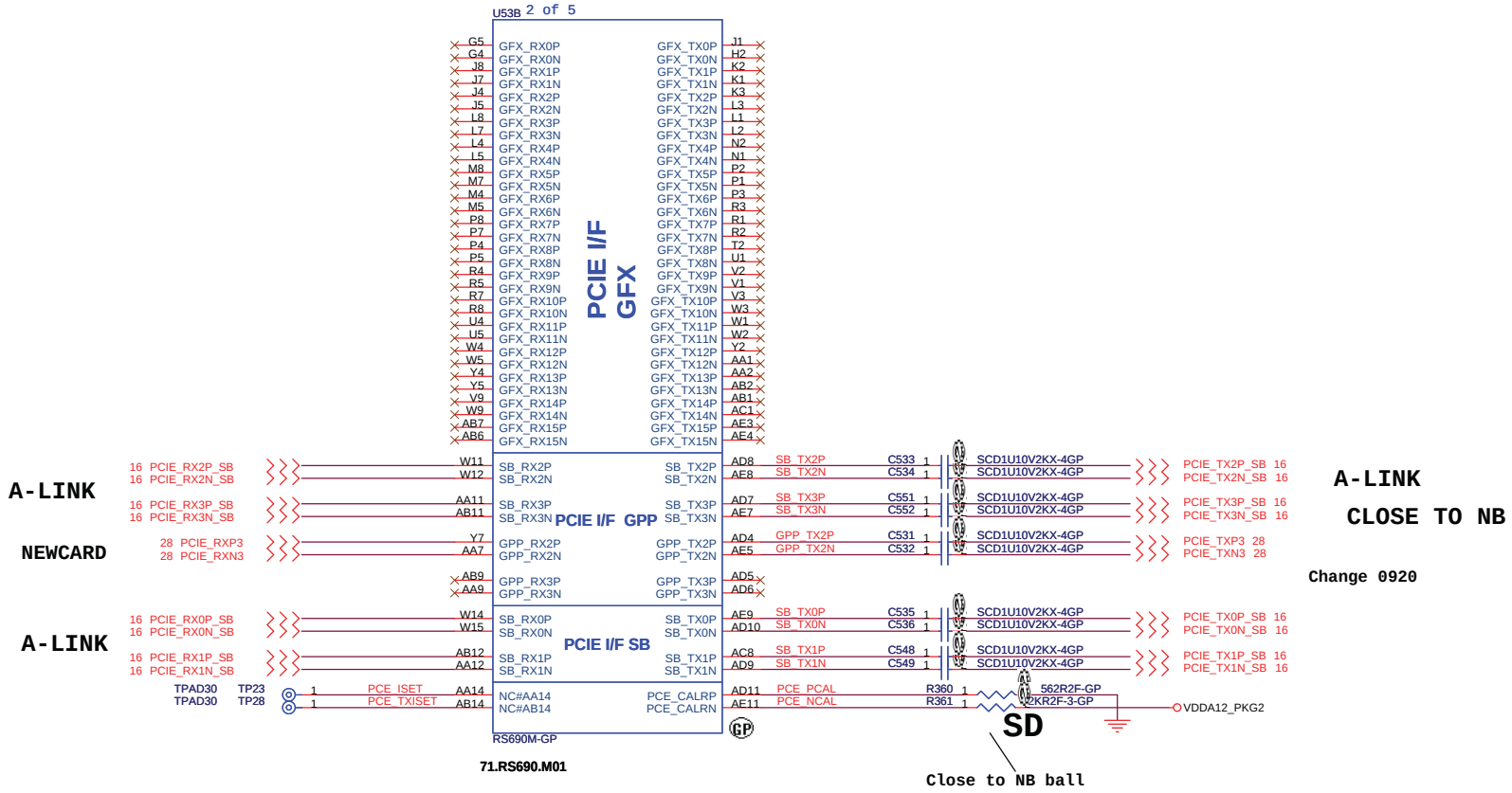
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_HT

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 10 of 46



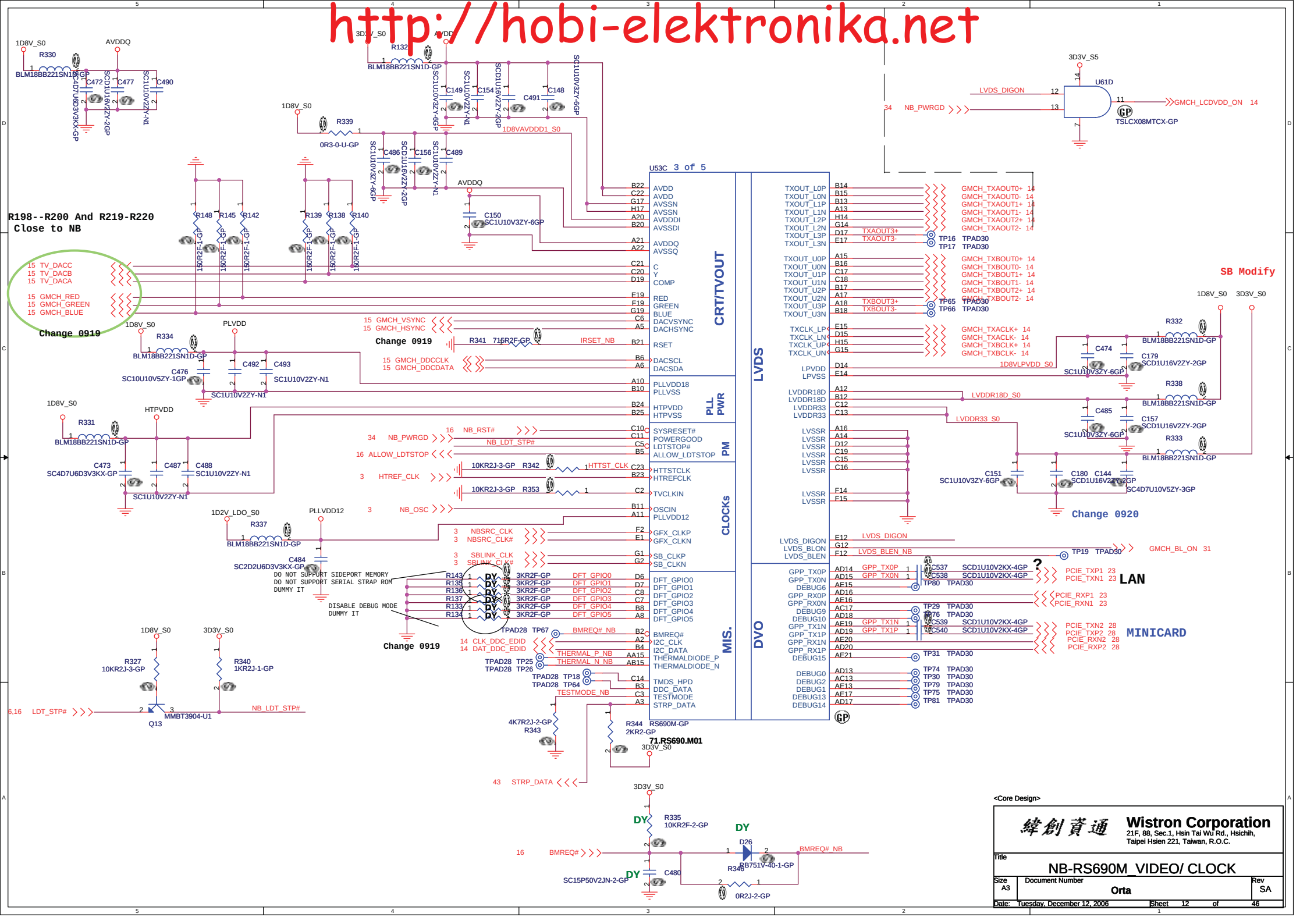
<Core Design>

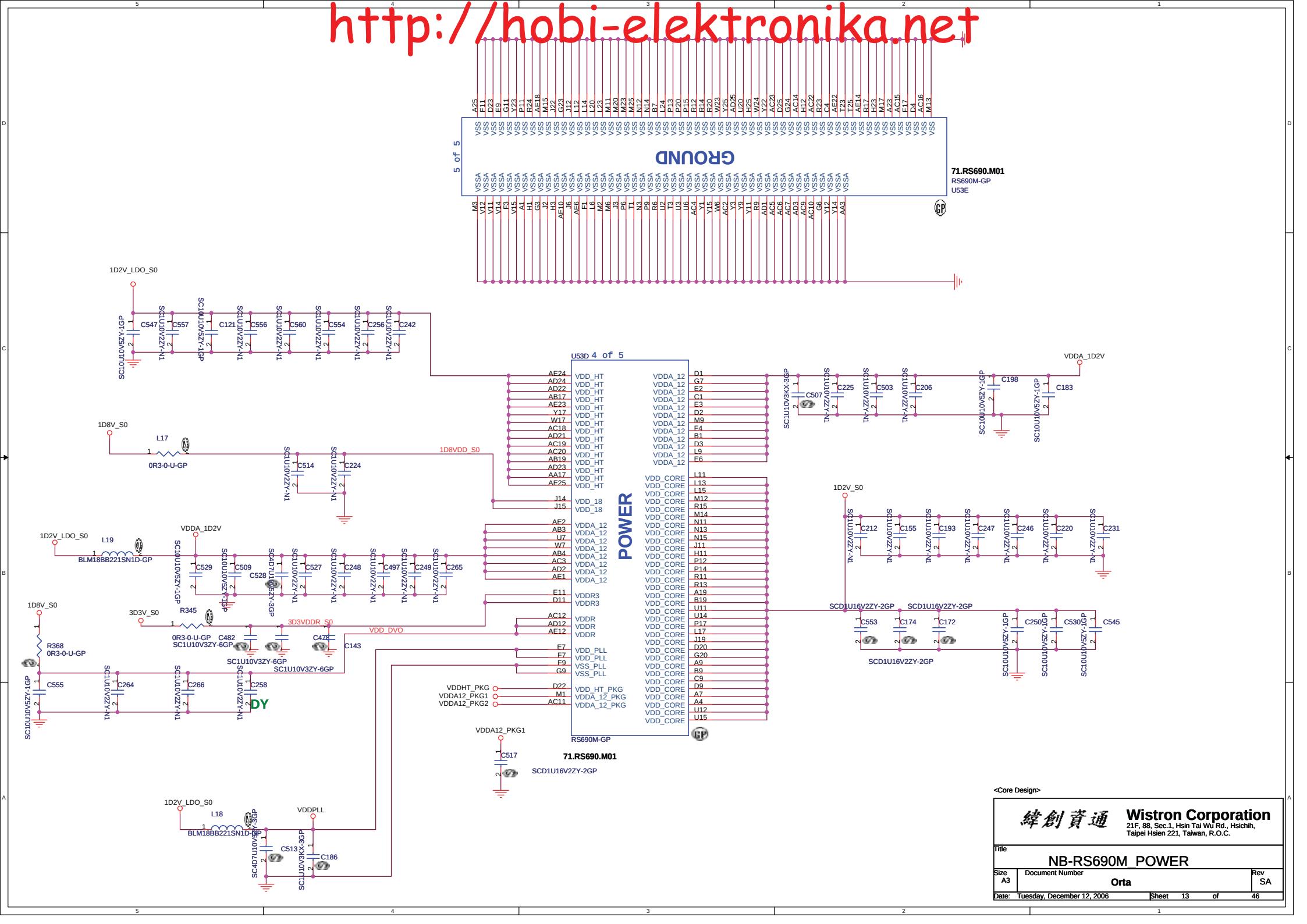
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_MEM/PCIE_LINK I/F

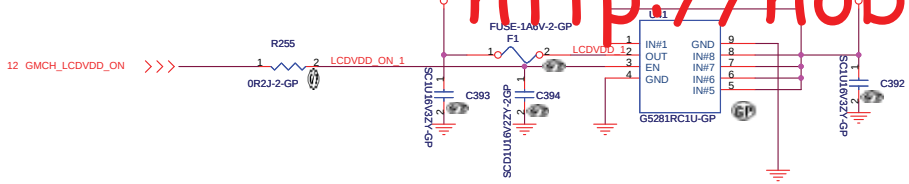
Size: A3 | Document Number: Orta | Rev: SA

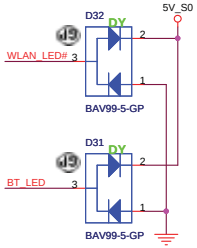
Date: Tuesday, December 12, 2006 | Sheet 11 of 46

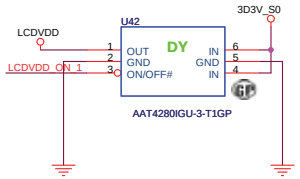


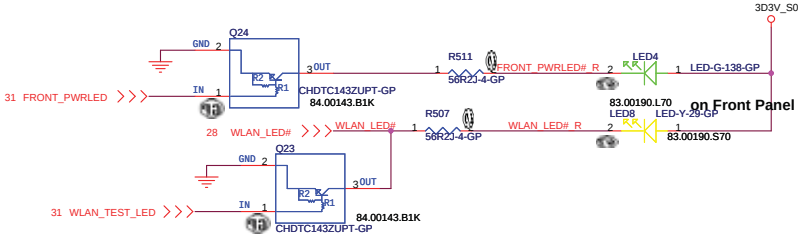


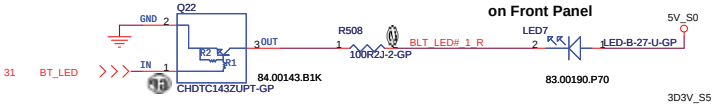
LCD/INVERTER CONN

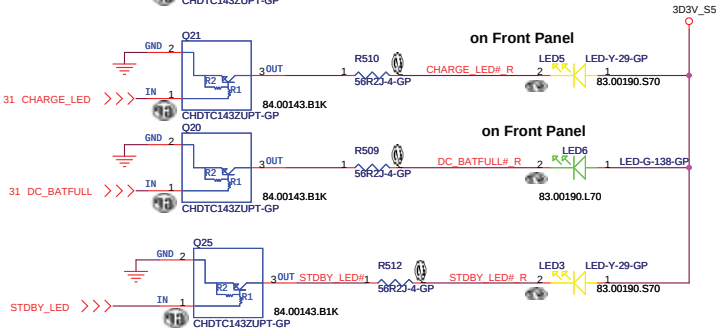


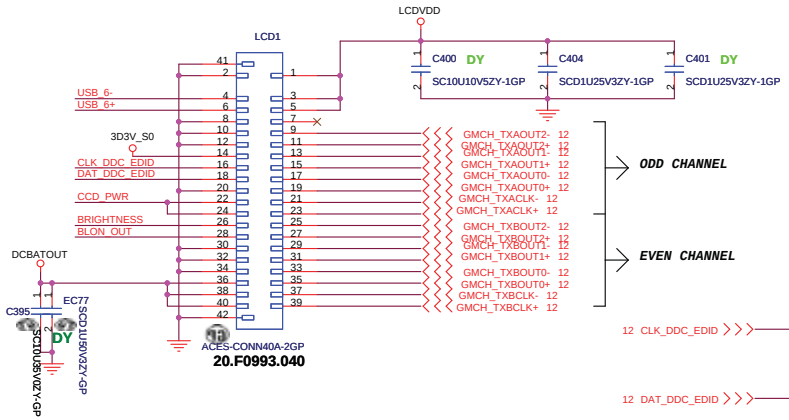


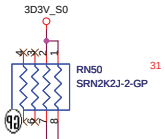


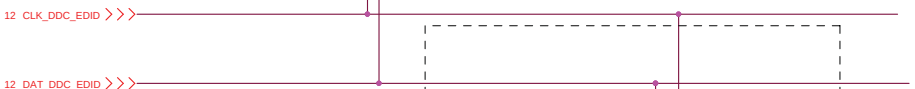


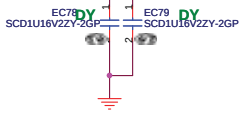


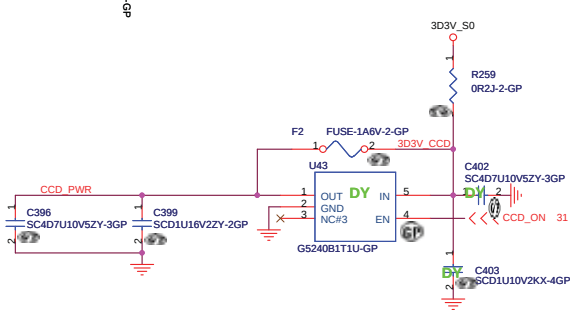


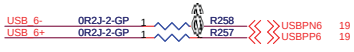


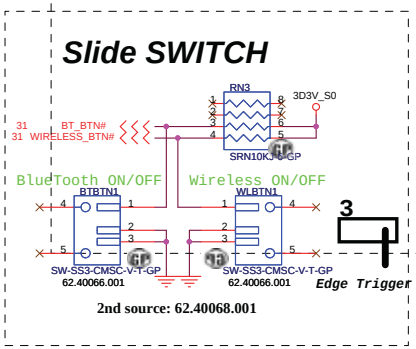




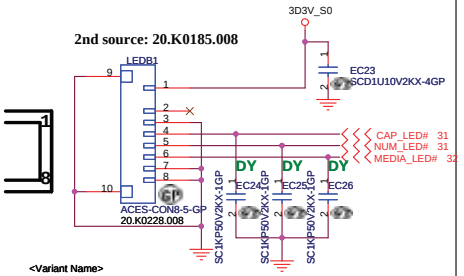






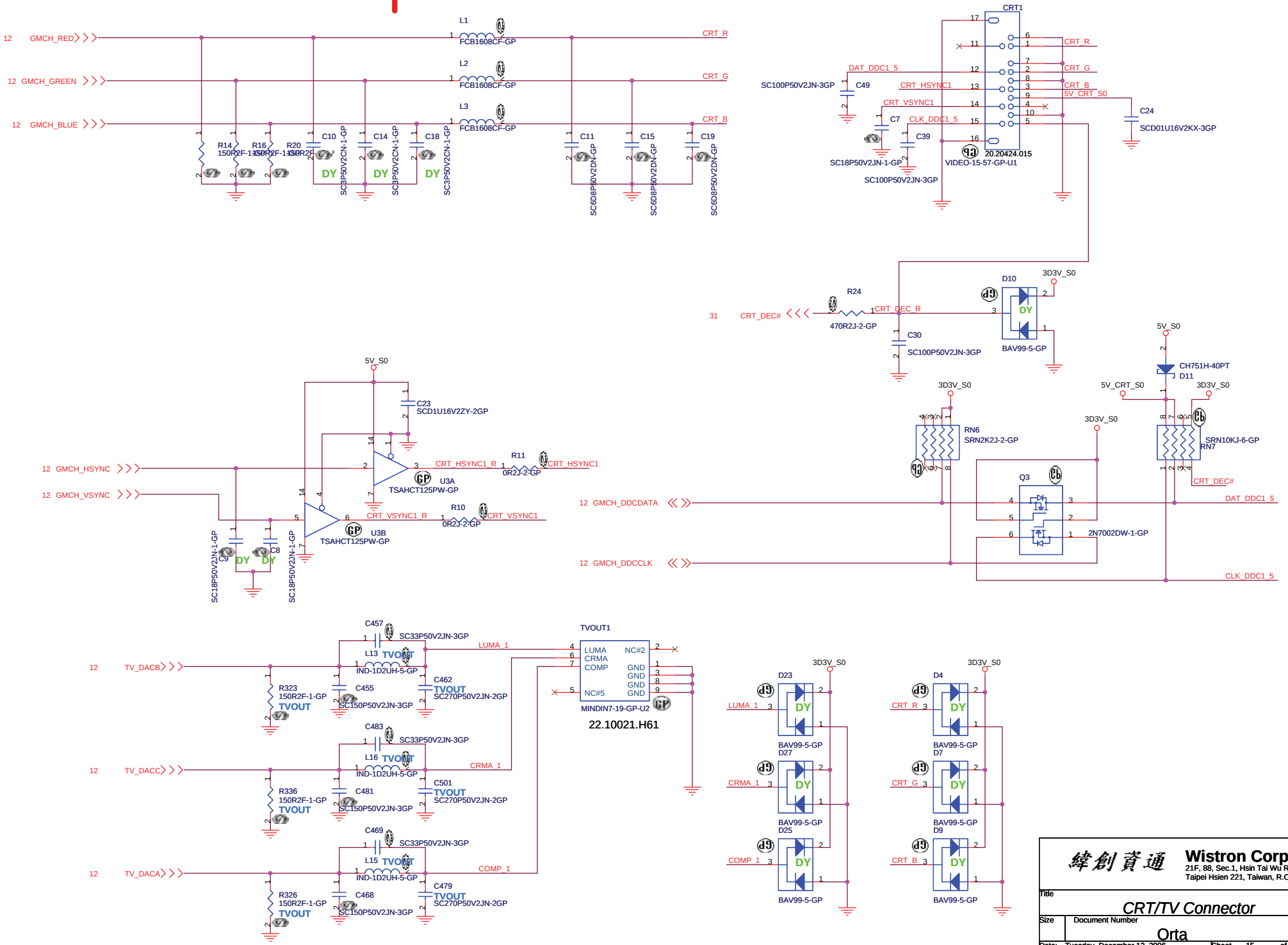


LED BD



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD CONN & LED	
Size	Document Number Orta	Rev SA
Date: Tuesday, December 12, 2006	Sheet 14 of 46	



緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*CRT/TV Connector*
Size	Document Number: Orta
Rev	SA
Date: Tuesday, December 12, 2006	Sheet 15 of 46

Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.

SB600 asserts PLTRST# to reset
devices on the platform.

Change 0921

PCIRST

U57A 1 of 4

SB600-GP

71.SB600.00U

2nd source: 20.D0198.103

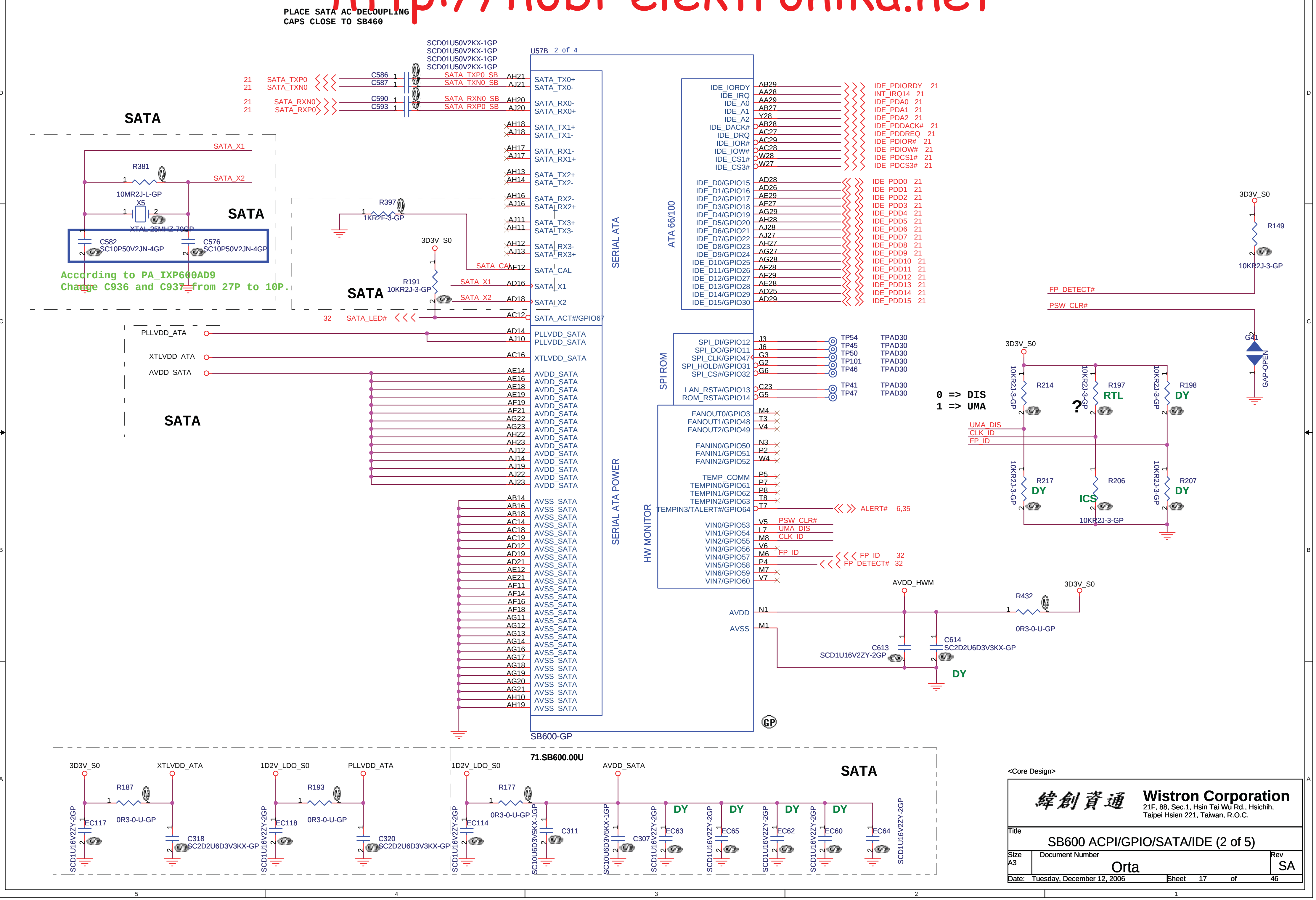
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 PCI/CPU/LPC/RTC (1 of 5)

Size: A3 | Document Number: Orta | Rev: SA

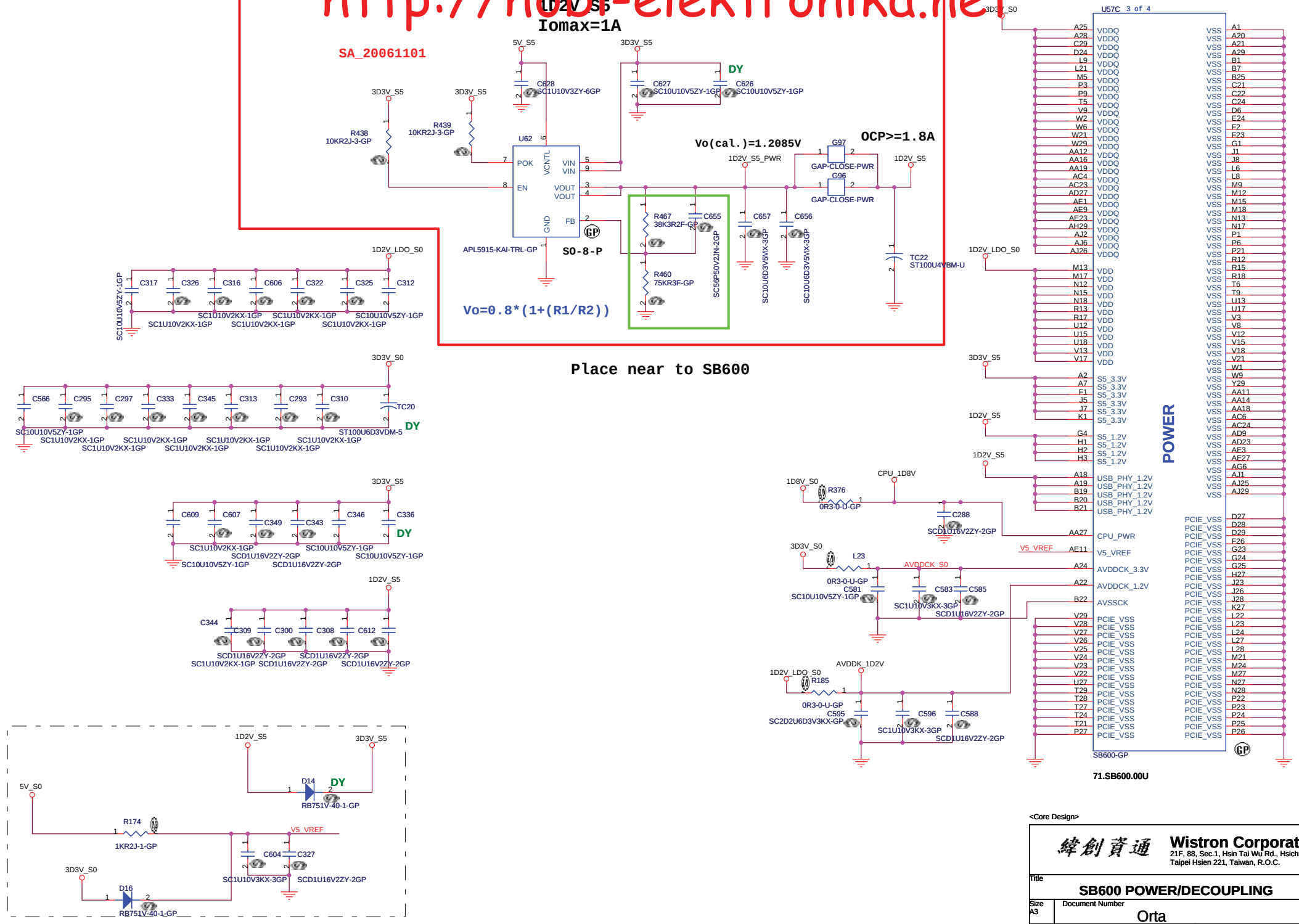
Date: Tuesday, December 12, 2006 | Sheet 16 of 46



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SB600 ACPI/GPIO/SATA/IDE (2 of 5)
Size	A3
Document Number	Orta
Rev	SA
Date	Tuesday, December 12, 2006
Sheet	17 of 46



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SB600 POWER/DECOUPLING	
Size A3	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 18 of 46	

11/02,
DUMMY refer to
ATI reference circuit
ver1.1

Change 0921

Change 0920

GPIO1 Has Internal
Pull-Up To 3.3V_S0

Change 0919;

Change 0919;

SB

NEWCARD /GLAN

DUMMY FOR
SB600
VER.A21

SPEC change

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	FT
4	BLUETOOTH
5	USB3
6	WEBCAM
7	USB4(Card Reader BD)
8	MINICARD
9	NEW1

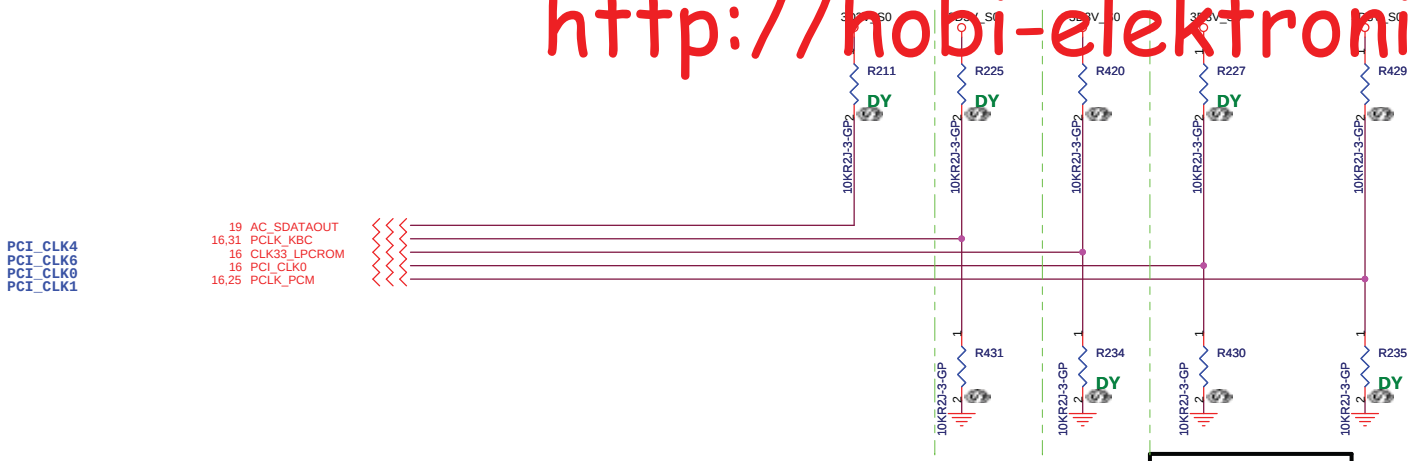
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 AC97/USB

Size: A3 | Document Number: Orta | Rev: SA

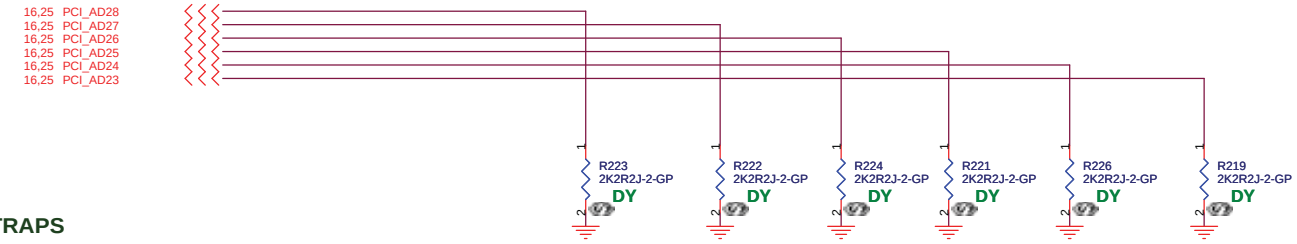
Date: Tuesday, December 12, 2006 | Sheet 19 of 46



REQUIRED SYSTEM STRAPS

				SB600	
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

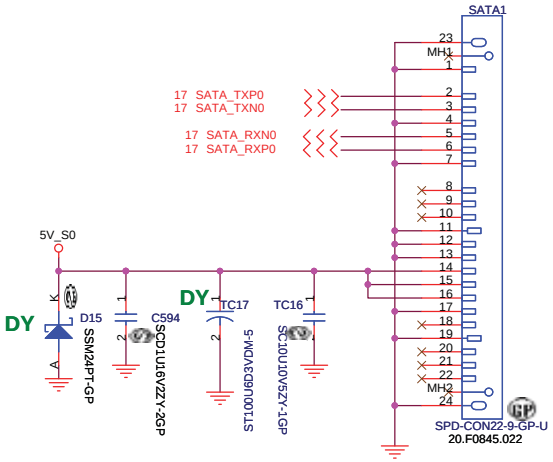
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 STRAPPING PIN

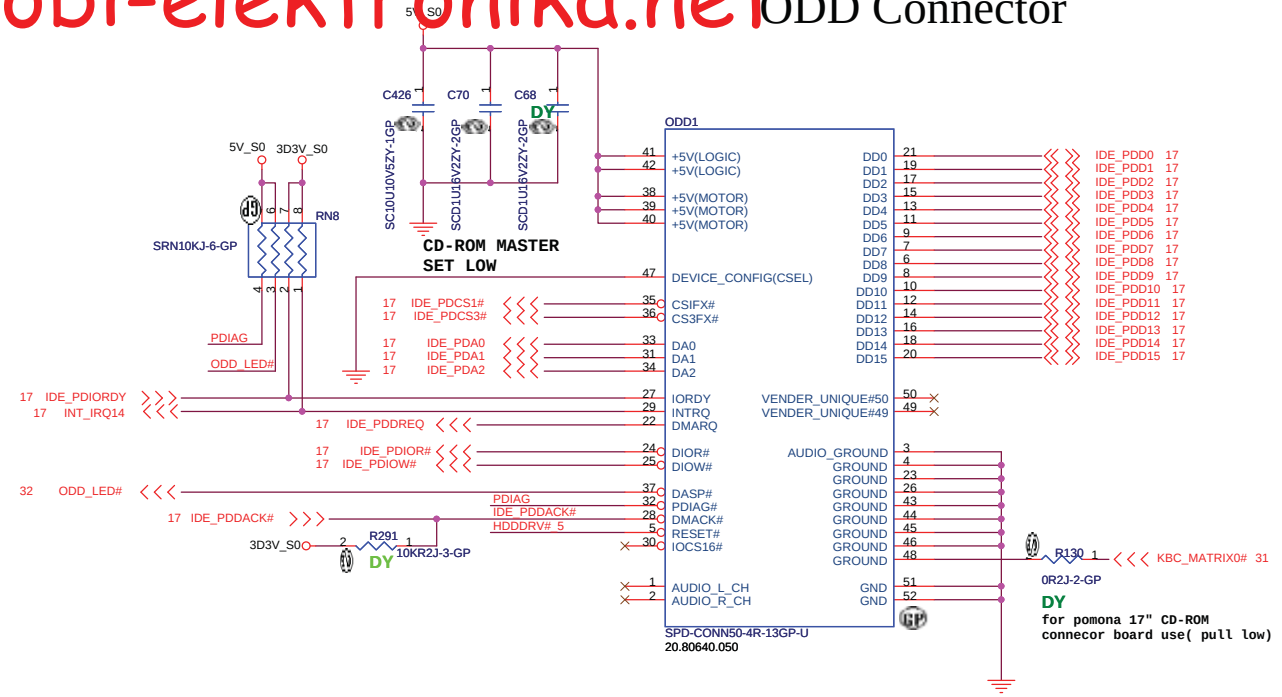
Size: A3 | Document Number: Orta | Rev: SA

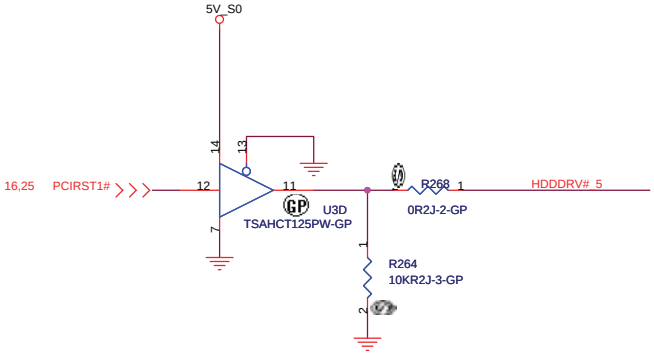
Date: Tuesday, December 12, 2006 | Sheet 20 of 46

SATA HD Connector



ODD Connector





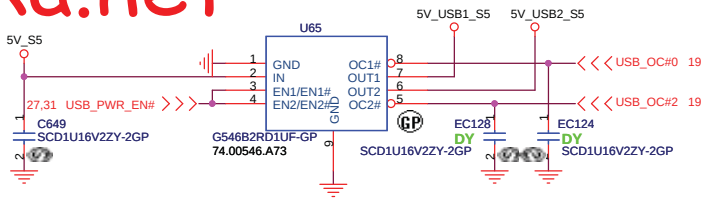
bom1

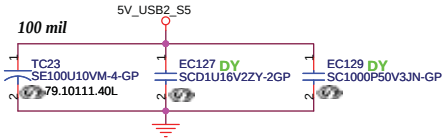
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

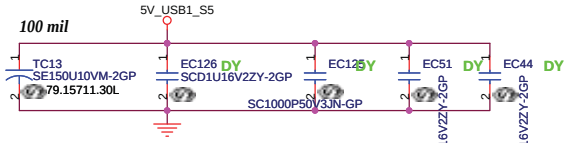
Title: HDD and CDROM

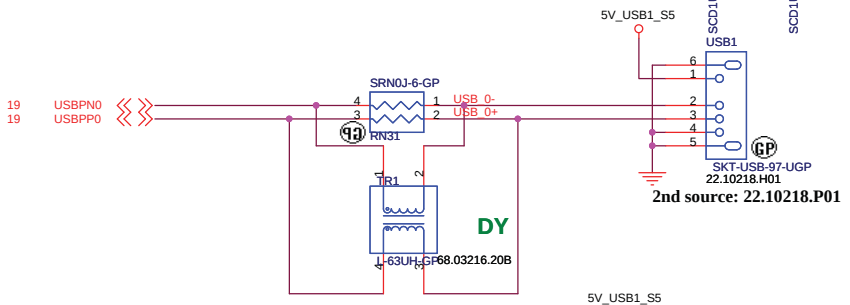
Size	Document Number	Rev
	Orta	SA

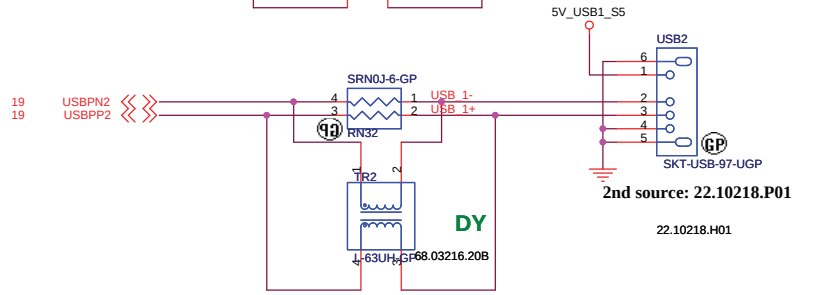
Date: Tuesday, December 12, 2006 Sheet 21 of 46

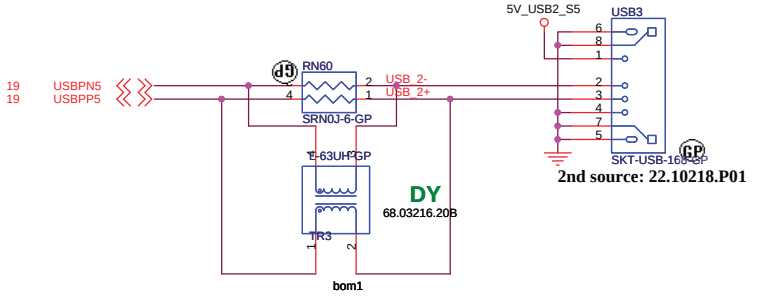




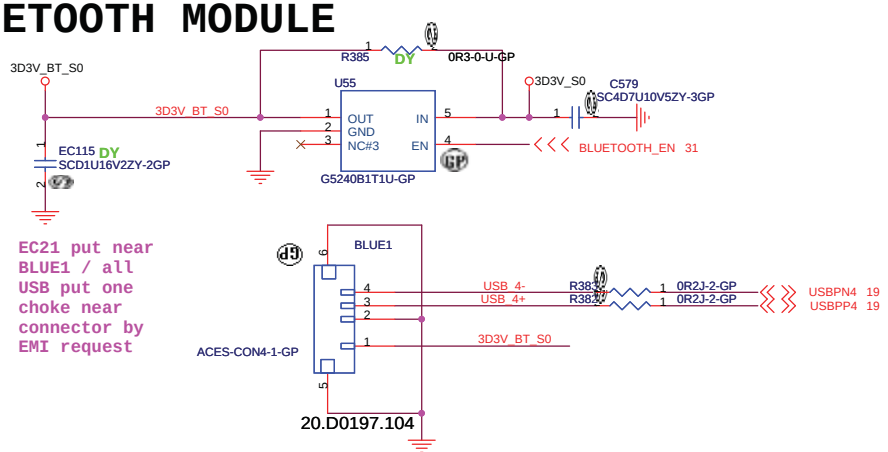




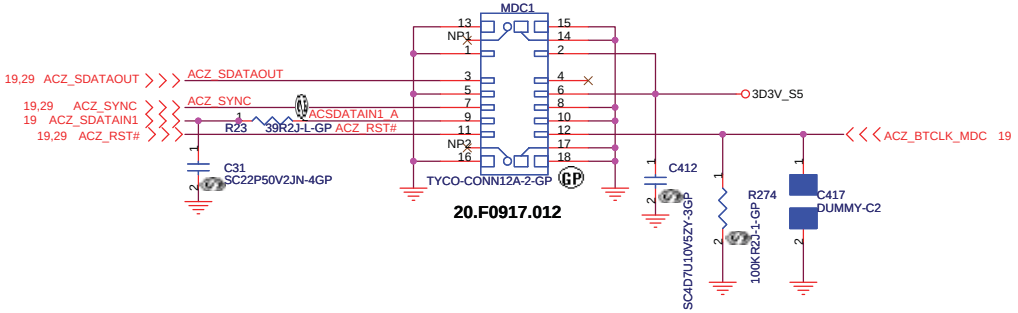




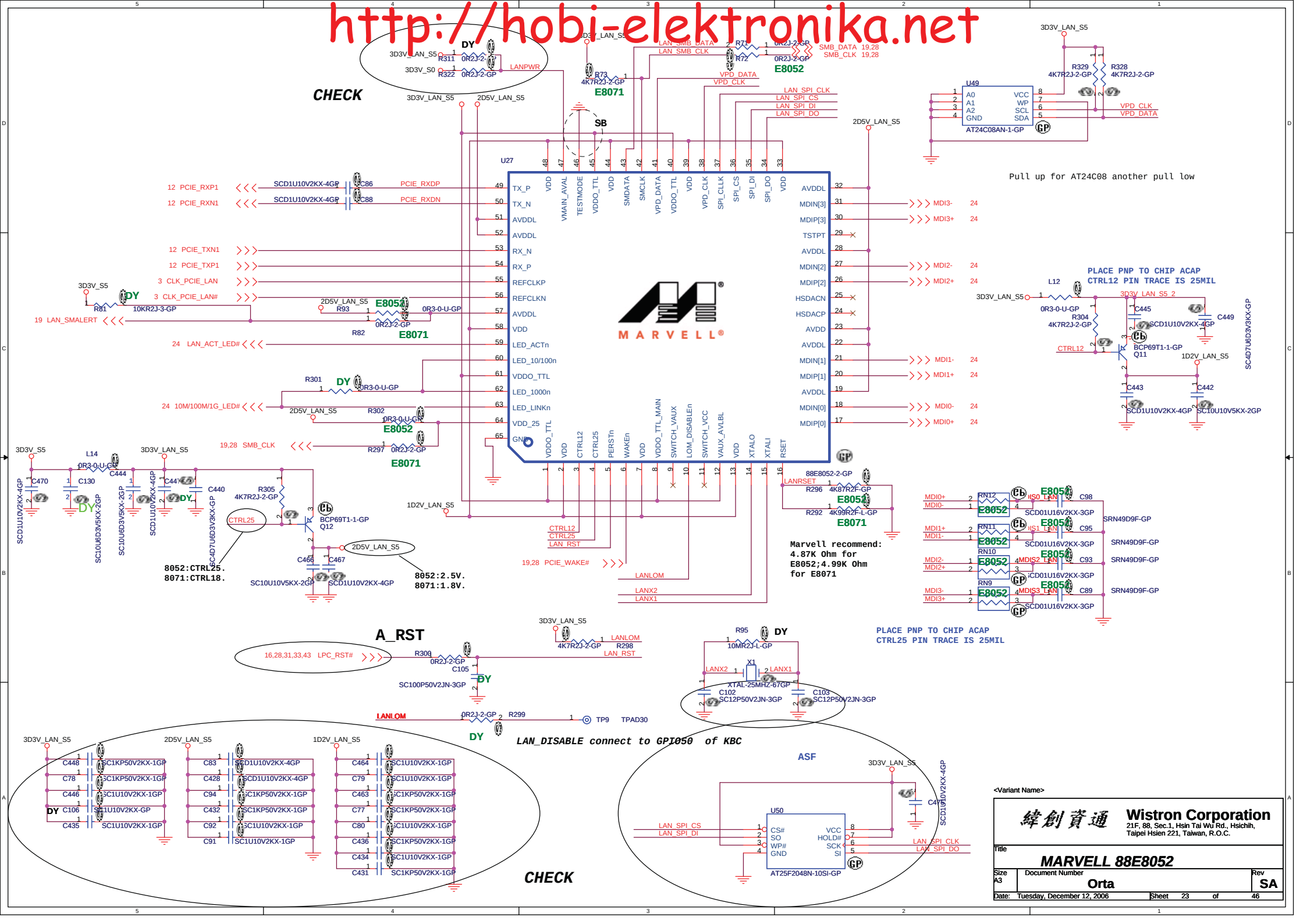
BLUETOOTH MODULE



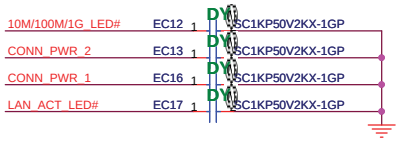
MDC 1.5 CONN

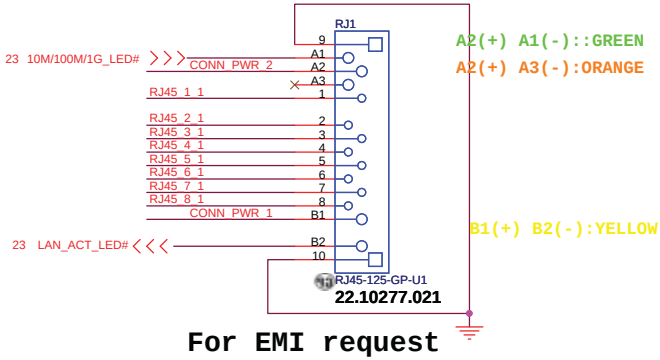


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **USB / MDC / BLUETOOTH**		
Size	Document Number: **Orta**	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 22 of 46	

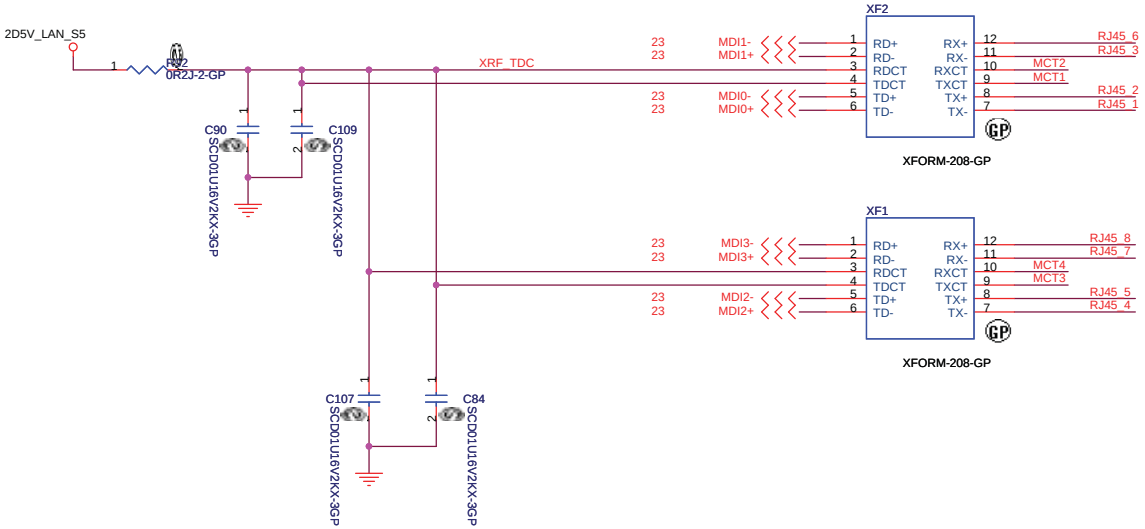


LAN Connector

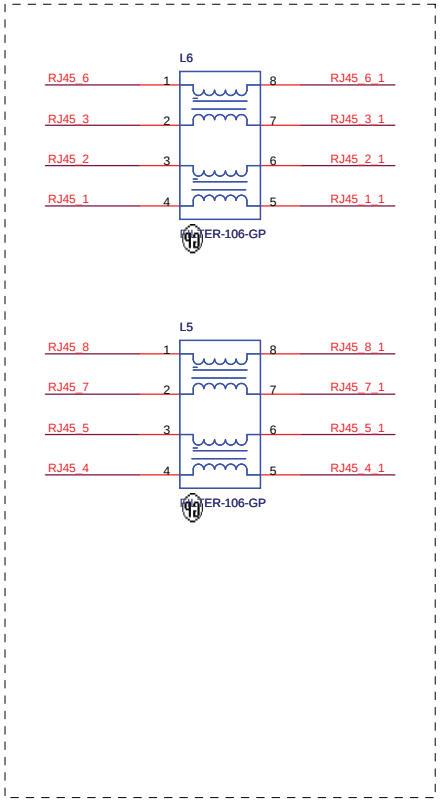




GIGA Lan Transformer



For EMI request

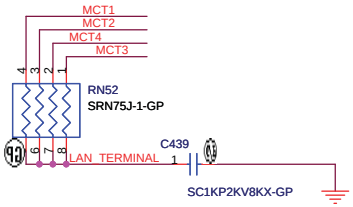


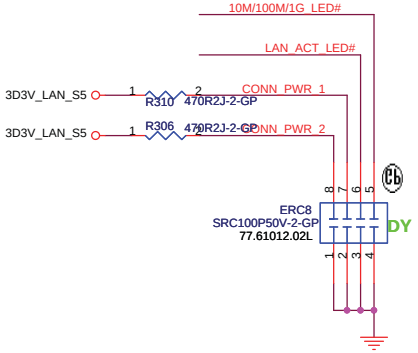
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6





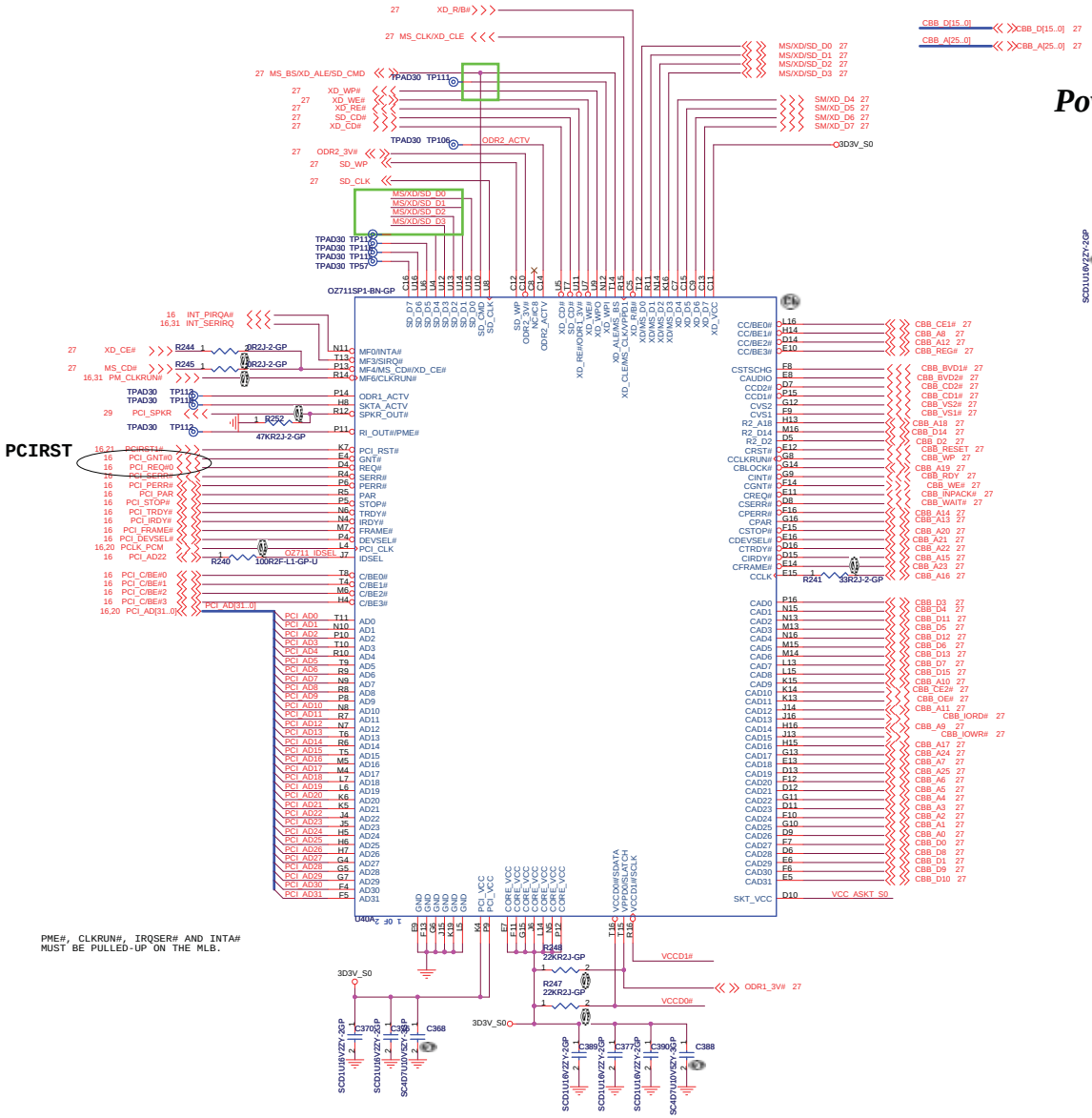
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

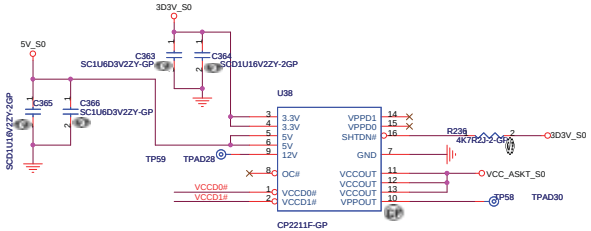
Title: **LAN Connector**

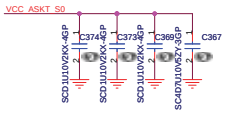
Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 24 of 46

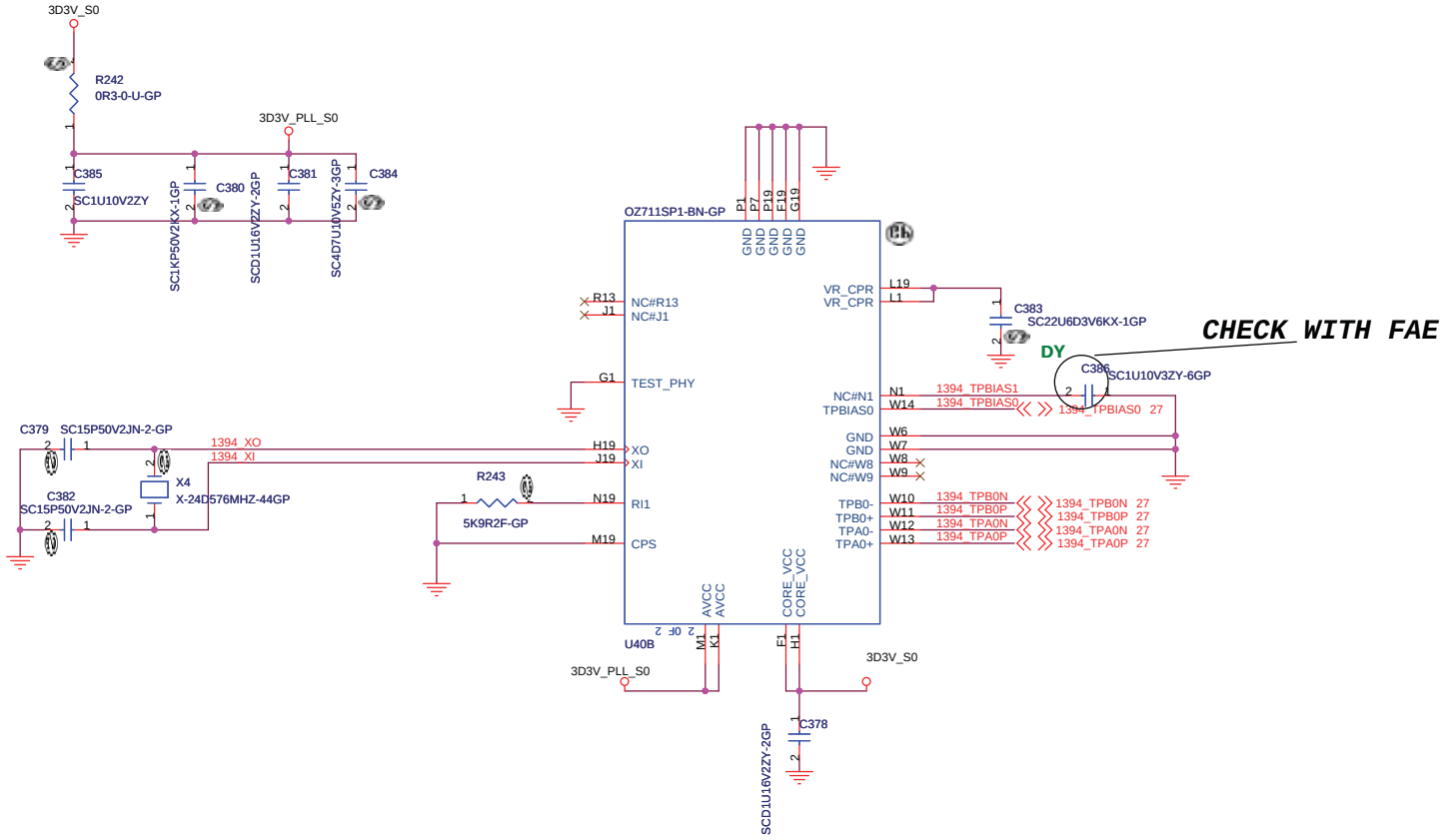


Power switch





<Variant Name>			
蜂創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	OZ711SP1 (1 of 2)		
Size	Document Number: Orta		Rev: SA
Date: Tuesday, December 12, 2006	Sheet 25 of 46		



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *OZ711SP1 (2 of 2)*

Size	Document Number	Rev
	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 26 of 46

PCMCIA Socket

Cardbus I/F

CBB_D[15..0] CBB_D[15..0] 25
CBB_A[25..0] CBB_A[25..0] 25

CBB_IORD# 25
CBB_IOWR# 25
CBB_OE# 25
CBB_WE# 25
CBB_REG# 25
CBB_RDY 25
CBB_WP 25
CBB_RESET 25
CBB_WAIT# 25
CBB_INPACK# 25

CBB_CE1# 25
CBB_CE2# 25
CBB_BVD1# 25
CBB_BVD2# 25
CBB_CD1# 25
CBB_CD2# 25
CBB_VS1# 25
CBB_VS2# 25

CN1
NP1
CBB_D3 CBB_D4 CBB_D11 CBB_D5 CBB_D12 CBB_D6 CBB_D13 CBB_D7 CBB_D14 CBB_D15
CBB_CD1# CBB_CE1# CBB_A10 CBB_CE2# CBB_OE# CBB_VS1# CBB_A11 CBB_IORD# CBB_A9 CBB_IOWR# CBB_A8 CBB_A17 CBB_A13 CBB_A18 CBB_A14 CBB_A19 CBB_WE# CBB_A20 CBB_RDY CBB_A21 CBB_A16 CBB_A22 CBB_A15 CBB_A23 CBB_A12 CBB_A24 CBB_A7 CBB_A25 CBB_A6 CBB_VS2# CBB_A5 CBB_RESET CBB_A4 CBB_WAIT# CBB_A3 CBB_INPACK# CBB_A2 CBB_REG# CBB_A1 CBB_BVD2# CBB_A0 CBB_BVD1# CBB_D0 CBB_D8 CBB_D1 CBB_D9 CBB_D2 CBB_D10 CBB_WP CBB_CD2#
PCMCIA
NP2
CARDBUS68P-11-GP-U1
62.10024.601

VCC_ASKT_S0
PCMCIA
C358 SC4D7U10V5ZY-3GP
C356 SC1K/50V2KX-1GP
C360 SCD1U25V3ZY-1GP
C351 SCD1U25V3ZY-1GP
C348 SC4D7U10V5ZY-3GP
C334 DY SCD01U16V2KX-3GP

Place close to pin 19.
C340 DUMMY-C2

Clock AC termination
33MHz clock for 32-bit Cardbus card I/F

PC1 PCMCIA
21.H0056.011 ICARDBUS-SKT42
2nd source: 21.H0140.001

CLOSE TO CHIP

1394_TPB0P
1394_TPB0N
1394_TPA0P
1394_TPA0N
R253 1394 56R2J-4-GP
R254 1394 56R2J-4-GP
R250 1394 56R2J-4-GP
R251 56R2J-4-GP 1394
26 1394_TPBIAS0
1394_TPBIAS0
1394_TPB0
C391 1394 SC1U10V3ZY-6GP
C387 1394 SC220P50V3JN-GP
1394 R249 5K1R2-GP

3D3V_S0
R468 10KR2J-3-GP
D17 BAW56-7-F-GP
ODR1_3V# 25
ODR2_3V# 25

5V_S5
EC43 DY SCD1U16V2ZY-2GP
CRB1
MH1 MH2
20.F0084.040 AMP-CONN40-2-UGP
2nd source: 20.F0853.040

25 XD_RE#
22,31 USB_PWR_EN#
19 USB_OC#7
25 XD_CD#
25 XD_CE#
25 XD_R/B#
25 XD_WE#
25 SD_CLK
25 MS_CD#
25 MS_CLK/XD_CLE
25 MS_BS/XD_ALE/SD_CMD
25 SD_CD#
25 SD_WP
R245 0R2J-2-GP
26 1394_TPB0N
26 1394_TPB0P
31 1394_DETECT
XD_WP# 25
USBPN7 19
USBPP7 19
SM/XD_D4 25
SM/XD_D5 25
SM/XD_D6 25
SM/XD_D7 25
MS/XD/SD_D0 25
MS/XD/SD_D1 25
MS/XD/SD_D2 25
MS/XD/SD_D3 25
1394_TPA0N 26
1394_TPA0P 26

XD
MS / MS PRO
SD / SD IO / MMC

<Variant Name>

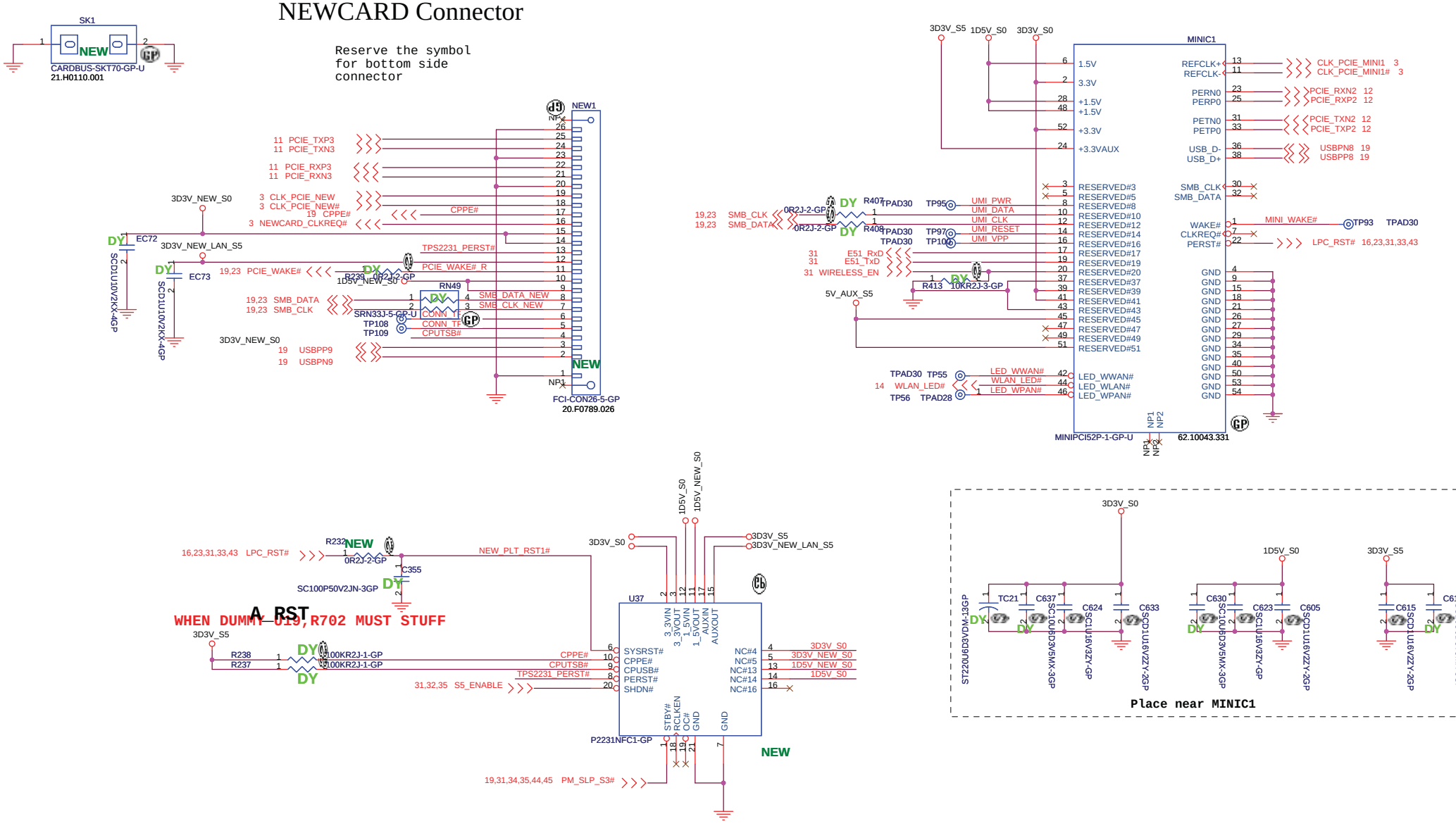
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER
Size: Document Number: Orta Rev: SA
Date: Tuesday, December 12, 2006 Sheet 27 of 46

Mini Card Connector

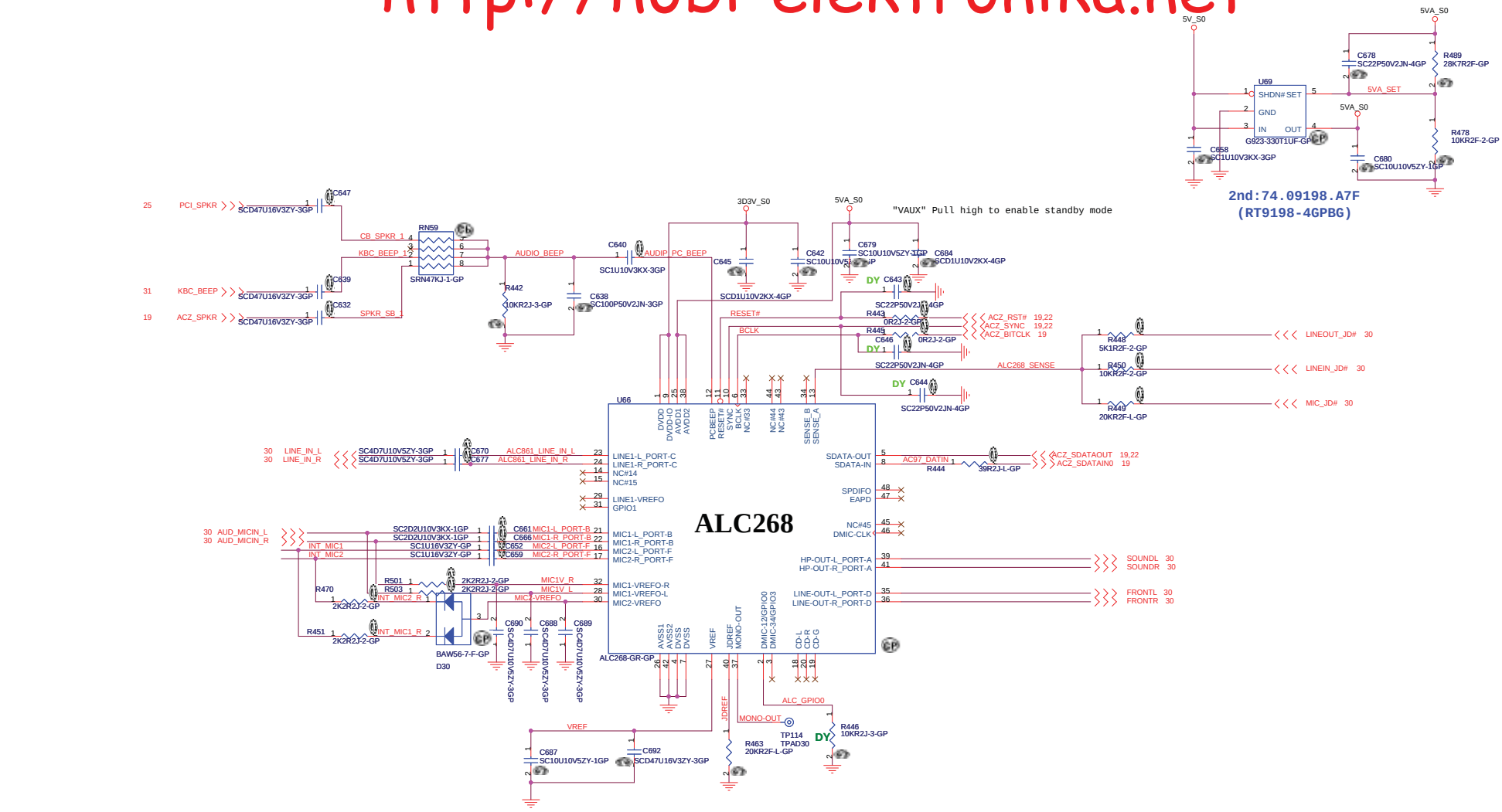
NEWCARD Connector

Reserve the symbol for bottom side connector

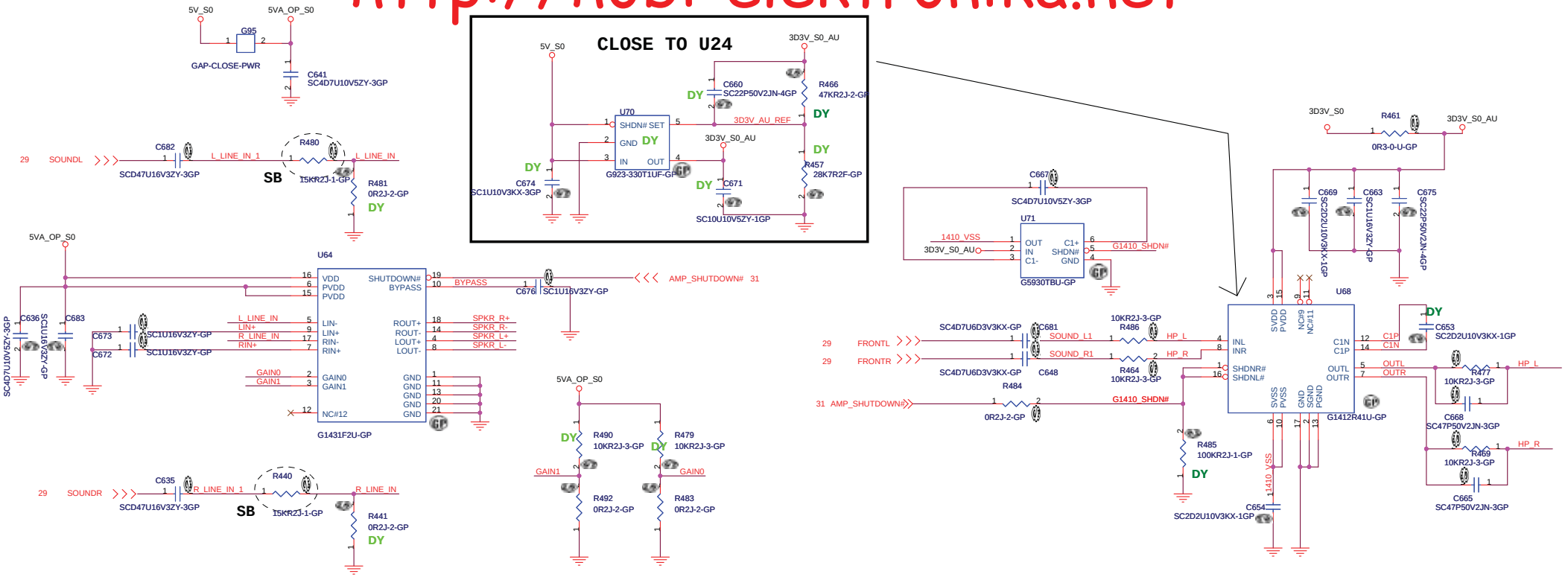


bom1

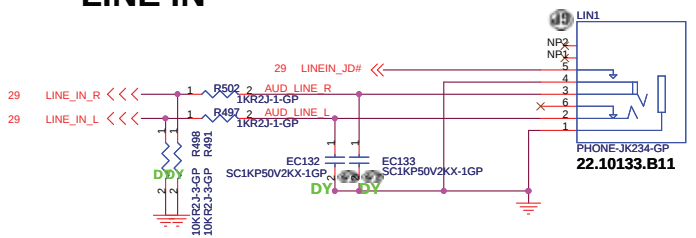
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD / NEW CARD		
Size	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 28 of 46	



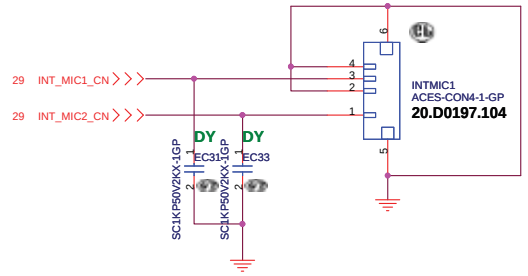
AUDIO AMP AMPLIFIER



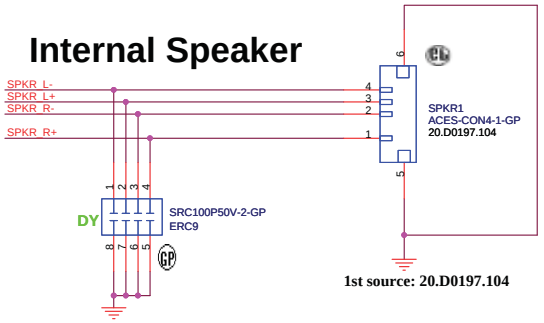
LINE IN



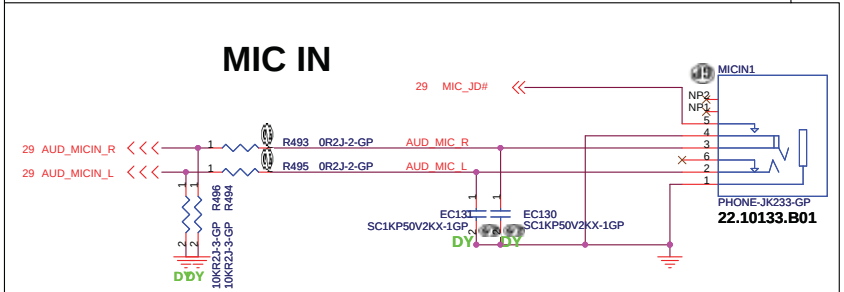
Internal Microphone



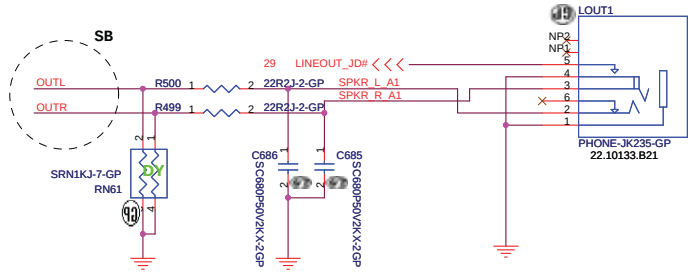
Internal Speaker



MIC IN

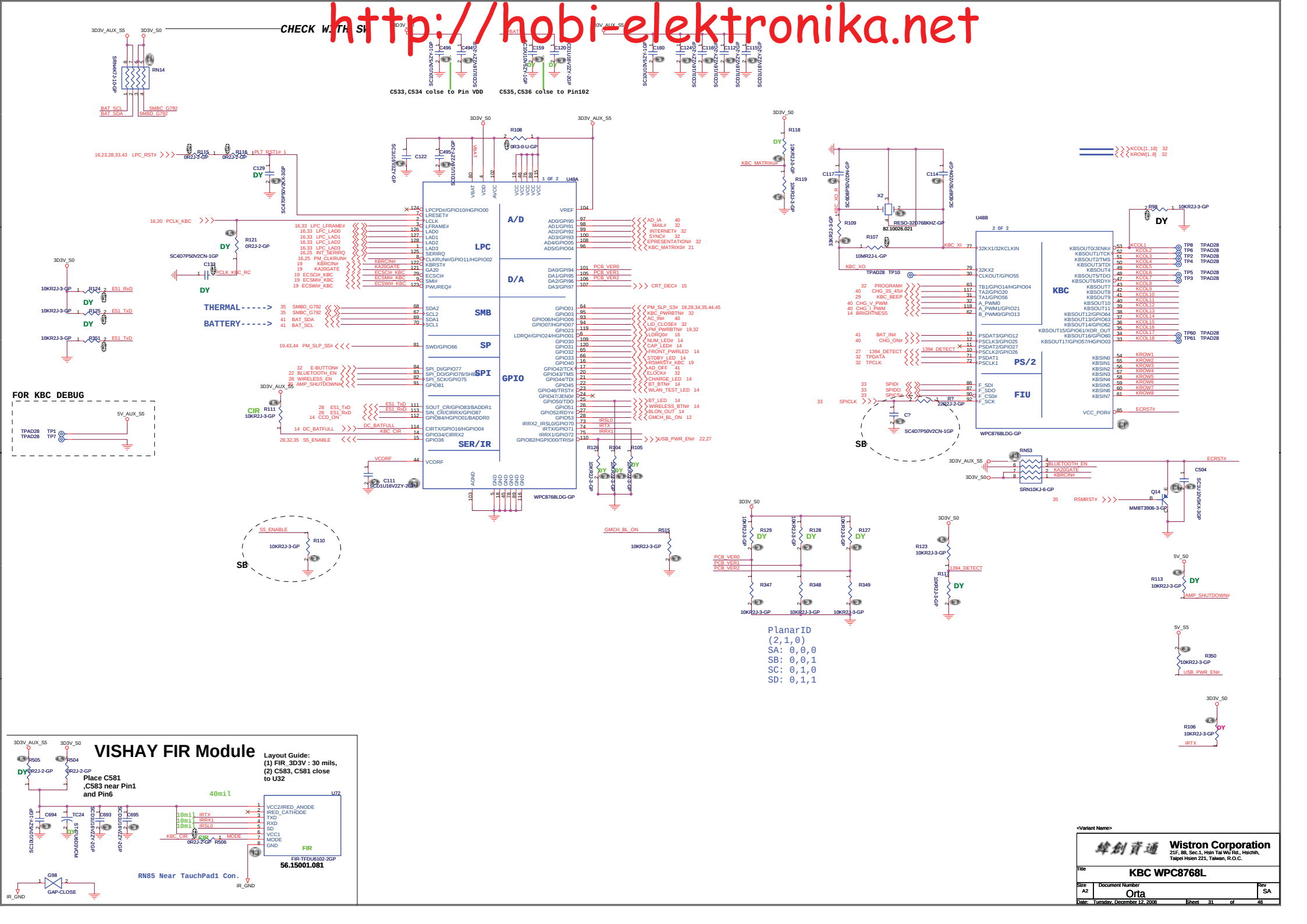


LINE OUT



<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO AMP AND JACK
Size	Document Number: Orta — Rev: SA
Date: Tuesday, December 12, 2006	Sheet 30 of 46



Internet Button / Mail Button

INTERNET1 / MAIL1
SW-TACT-91-GP
62.40009.561

RN5
SRN10KJ-6-GP

MAIL# 1
INTERNET# 1
Program 1
E-Button 1

Cover Up Switch

2nd source:20.F00984.002

LID1
ACES-CON2-GP-U

R8 10KR2J-3-GP
R9 100R2F-L1-GP-U
C6 SCD22U16V3KX-2-GP

COVER_SW#
LID_CLOSE# 31

Program Button / E-Button

PROGRAM1 / EBUTTON1
SW-TACT-91-GP
62.40009.561

RN4 SRN470J-3-GP

MAIL# 31
INTERNET# 31
PROGRAM# 31
E-BUTTON# 31

ERC1 SRC1KP50V8MX-GP

Power Button

R7 10KR2J-3-GP
R6 470R2J-2-GP
C5 SCD1U16V2ZY-2GP

KBC_PWRBTN#
KBC_PWRBTN# 31

PWRSW1
SW-TACT-103-GP-U
62.40009.631

SYNC

SYNC1
SW-TACT-91-GP
62.40009.561

RN2 SRN10KJ-6-GP

SYNC# 1
EPRESENTATION# 1
ELOCK# 1

SYNC# 31
EPRESENTATION# 31
ELOCK# 31

RN1 SRN470J-3-GP

EPRESENTATION

EPRESENTATION1
SW-TACT-91-GP
62.40009.561

ELOCK

ELOCK1
SW-TACT-91-GP
62.40009.561

D24 BAW56PT-U
83.00056.E11

21 ODD_LED#
17 SATA_LED#
MEDIA_LED# 14

Check test point

3D3V_AUX_S5	TP69	TPAD30
3D3V_S5	TP62	TPAD30
5V_S5	TP71	TPAD30
19,31 PM_PWRBTN#	TP68	TPAD30
28,31,35 S5_ENABLE	TP63	TPAD30

Test Point放在Dimm Door打開可量測處

EMI Bypass cap.

ERC2 SRC100P50V-2-GP
ERC4 SRC100P50V-2-GP
ERC5 SRC100P50V-2-GP
ERC7 SRC100P50V-2-GP
ERC6 SRC100P50V-2-GP
ERC3 SRC100P50V-2-GP

KCOL14 KCOL15 KCOL16 KCOL8
KCOL10 KCOL6 KCOL7 KCOL5
KCOL4 KCOL3 KCOL2 KCOL1
KROW2 KROW6 KROW7 KROW8
KROW1 KROW3 KROW4 KROW5
KCOL11 KCOL12 KCOL13 KCOL9

20.K0127.026

KB1 ETY-CON26-2-GP

KCOL1 KCOL2 KCOL3 KCOL4 KCOL5 KCOL6 KCOL7 KCOL8 KCOL9 KCOL10 KCOL11 KCOL12 KCOL13 KCOL14 KCOL15 KCOL16 KCOL17 KCOL18
KROW1 KROW2 KROW3 KROW4 KROW5 KROW6 KROW7 KROW8

Internal KeyBoard CONN

1 25

CHECK KB SPEC. AND PIN DEFINE

20.K0228.012

RN22 SRN10KJ-6-GP
RN26 SRN100J-3-GP Morar_SB

EC30 EC29 C200 SCD1U16V2ZY-2GP
EC28 EC32 SC4750V2JN-3GP
EC20 EC19 SC100P50V2JN-3GP

TPDATA
TPCLK
TP_DATA
TP_CLK

TP_RIGHT
TP_SCROLL_RIGHT
TP_SCROLL_UP
TP_SCROLL_LEFT
TP_SCROLL_DOWN
TP_LEFT

TPAD1 ACES-CON12-4-GP

KROW[1..8] KROW[1..8] 31
KCOL[1..18] KCOL[1..18] 31

EC39 EC38 EC37 EC36 EC35 EC34 SC1KP50V2KX-1GP

20.K0228.015

FP1 ACES-CON15-GP

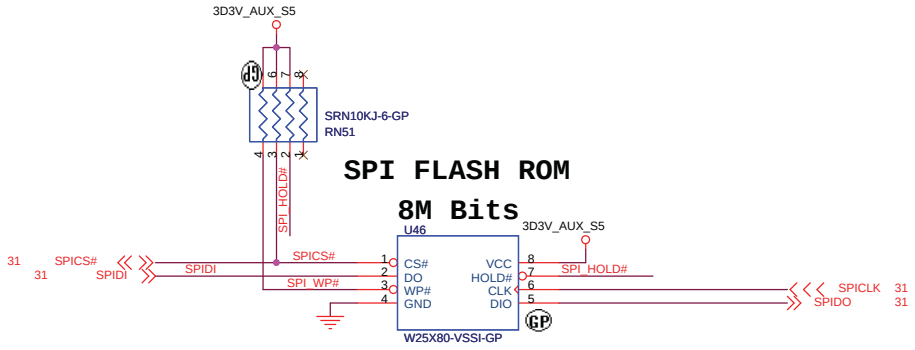
EC42 EC40 EC41 EC45 SCD1U16V2ZY-2GP
C233 C227 SC1U16V2ZY-GP
SC1KP50V2KX-1GP

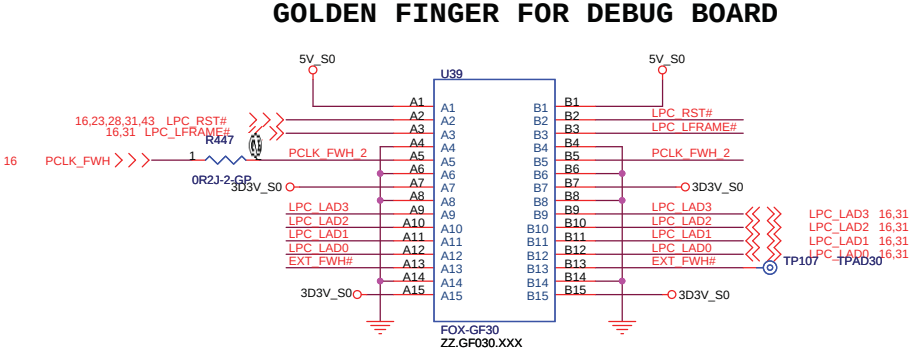
FP_DETECT#
FP_ID
USBPP3
USBPN3
R359 R358 0R2J-2-GP
USB 3+
USB 3-

TP_RIGHT
TP_SCROLL_RIGHT
TP_SCROLL_UP
TP_SCROLL_LEFT
TP_SCROLL_DOWN
TP_LEFT

bom1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BUTTONs / KB / TOUCHPAD
Size	Document Number: Orta — Rev: SA
Date: Tuesday, December 12, 2006	Sheet 32 of 46



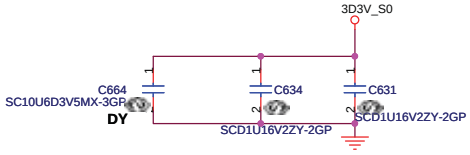


TOP VIEW

A15 (B1)
A14 (B2)
⋮ ⋮
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

```
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
```



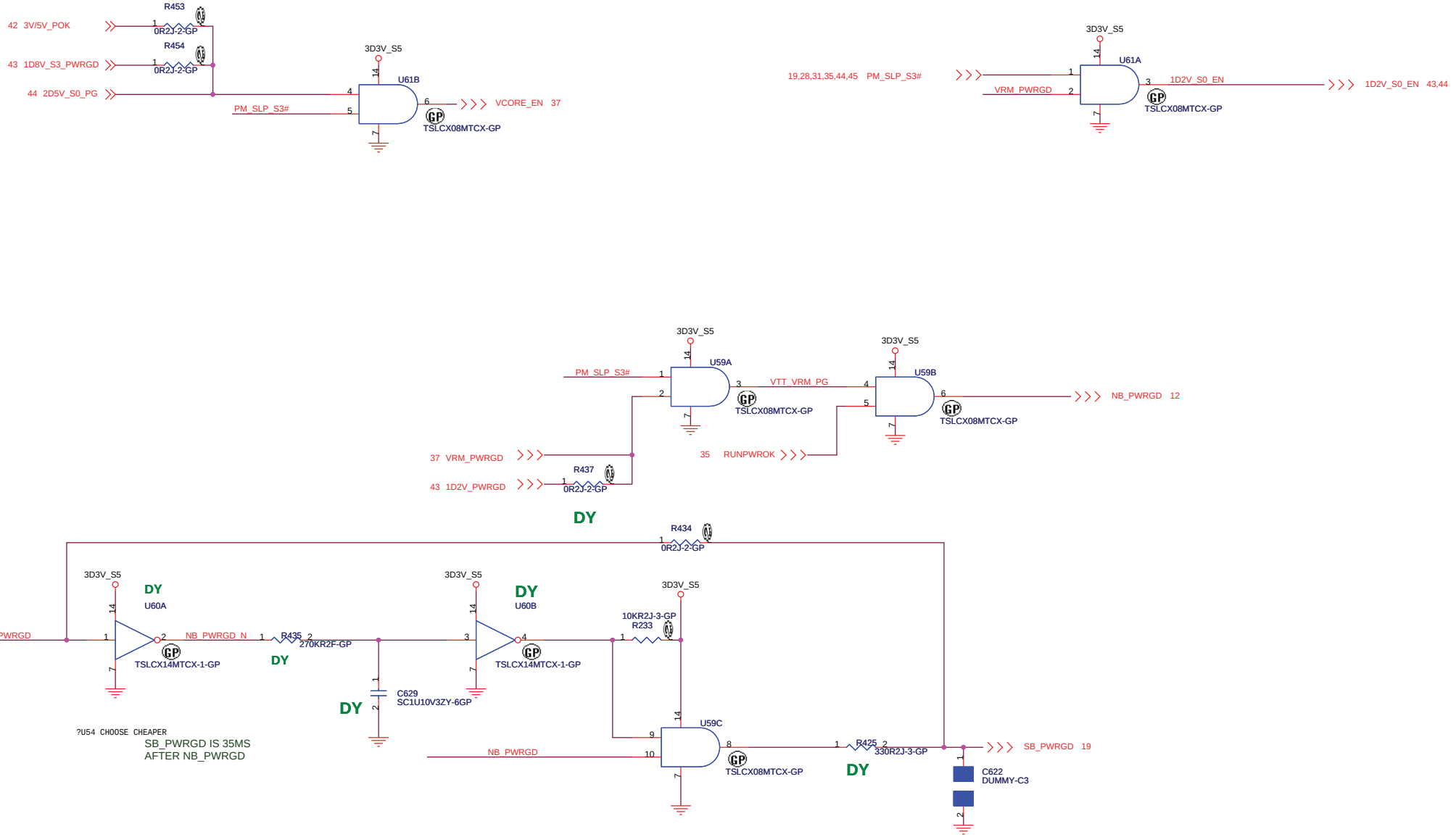
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 33 of 46



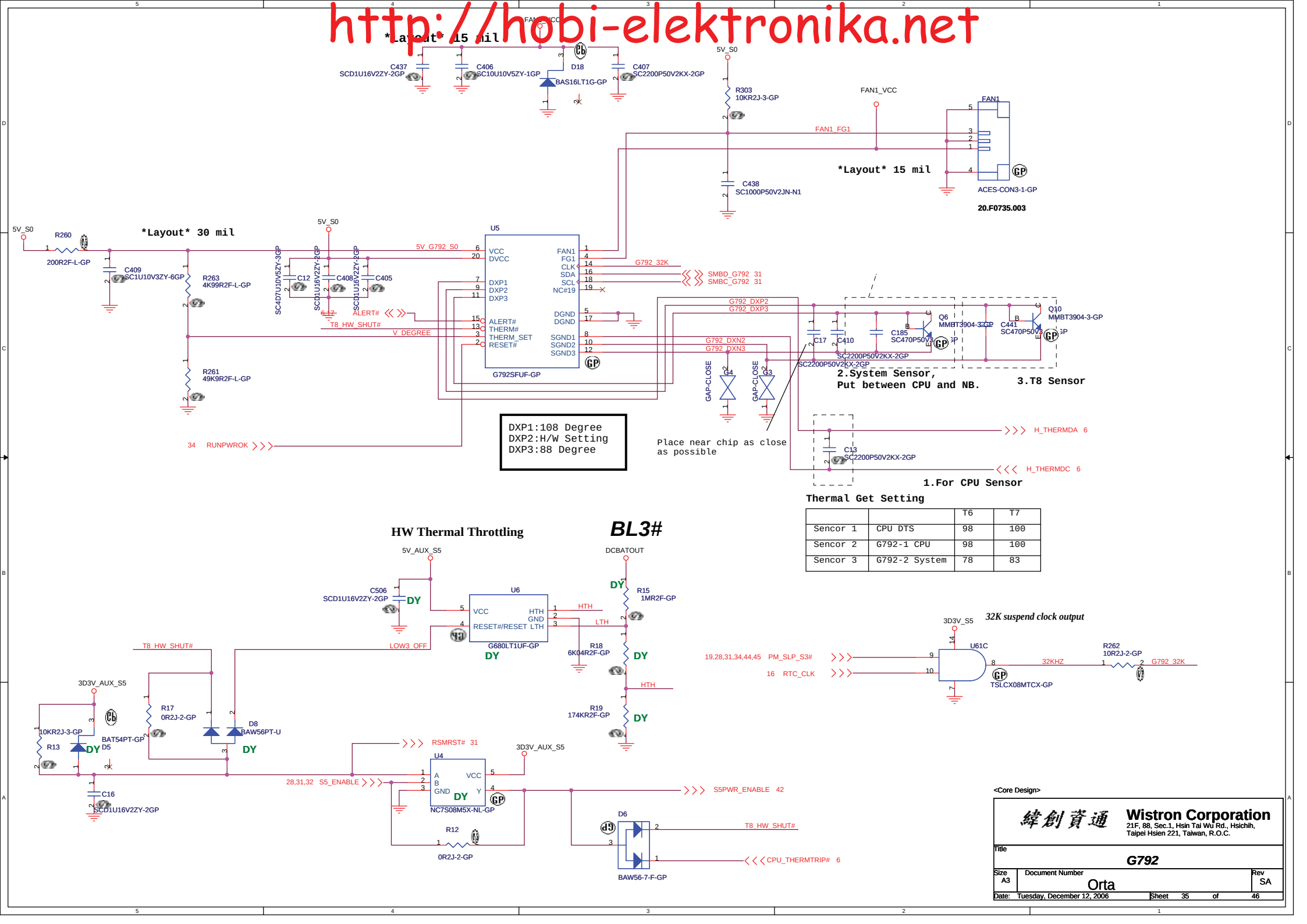
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES(1/2)

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 34 of 46



		T6	T7
Sencor 1	CPU DTS	98	100
Sencor 2	G792-1 CPU	98	100
Sencor 3	G792-2 System	78	83

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 35 of 46

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

COREFB
COREFB#

Input Power
VCC(I)
VCC(I)
VCC(I)

DCBATOUT
5V_S0
3D3V_S0

TI TPS51120
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

DCBATOUT_51120

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

APL5332KAC-TRLGP

Adapter

Input Signal
(I)

Output Signal
(O)

AD_OFF
AD_IN

Input Power
VCC(I)
VCC(I)

AD_JK
5V_AUX_S5

Output Power
VCC(O)

AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Input Power
DCIN (I)

AD+

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

Output Power
VCC(O)
VCC(O)

1.8V_S3
0.9V_S3

ISL6268_1D2V

1D2V_S0_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

5V_S5
DCBATOUT

Output Power
1D2V_PWR

1D2V (6.5A)

ISL6268_VGA_CORE

VGA_CORE_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

5V_S5
DCBATOUT

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

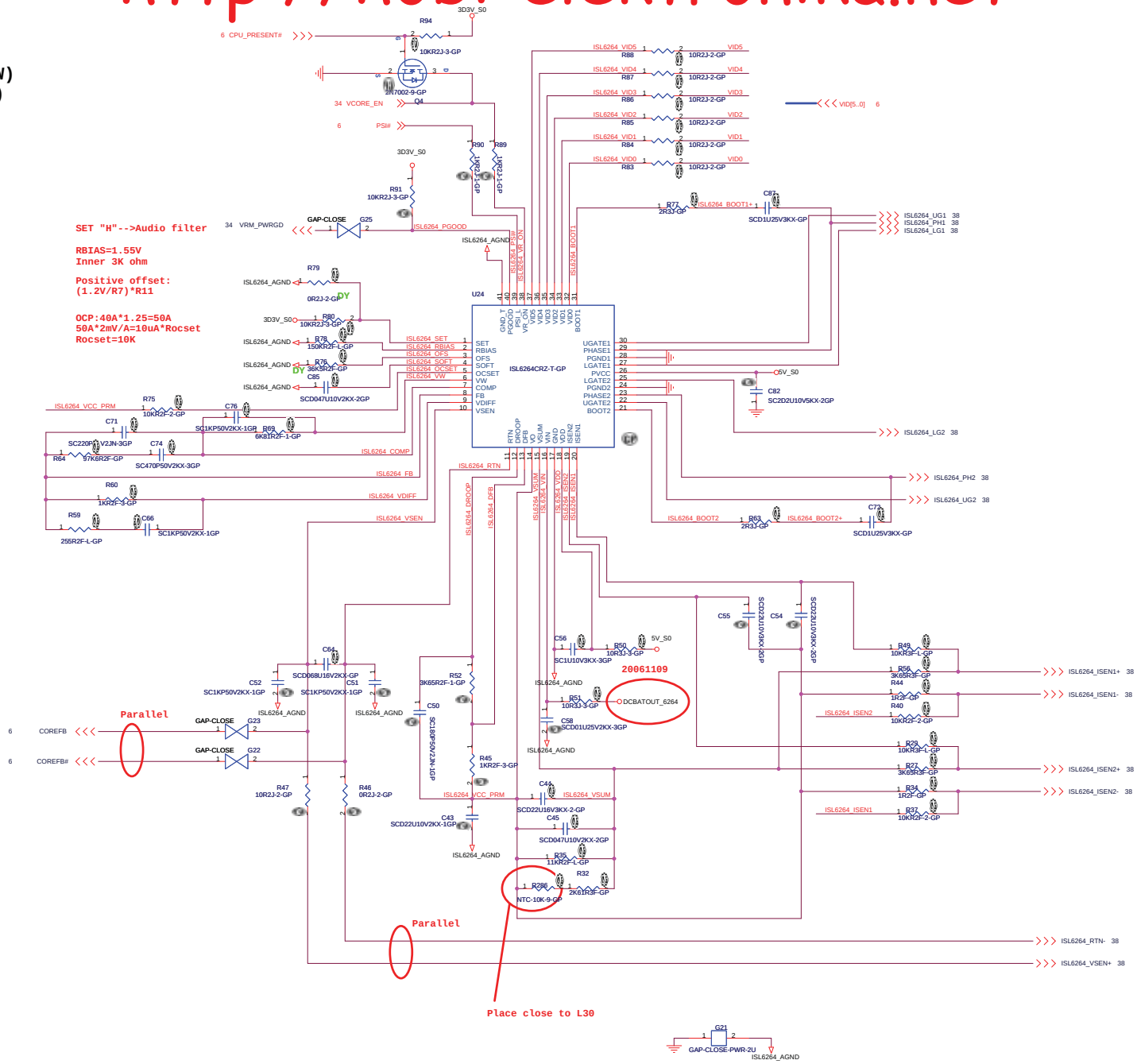
Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 36 of 46

CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



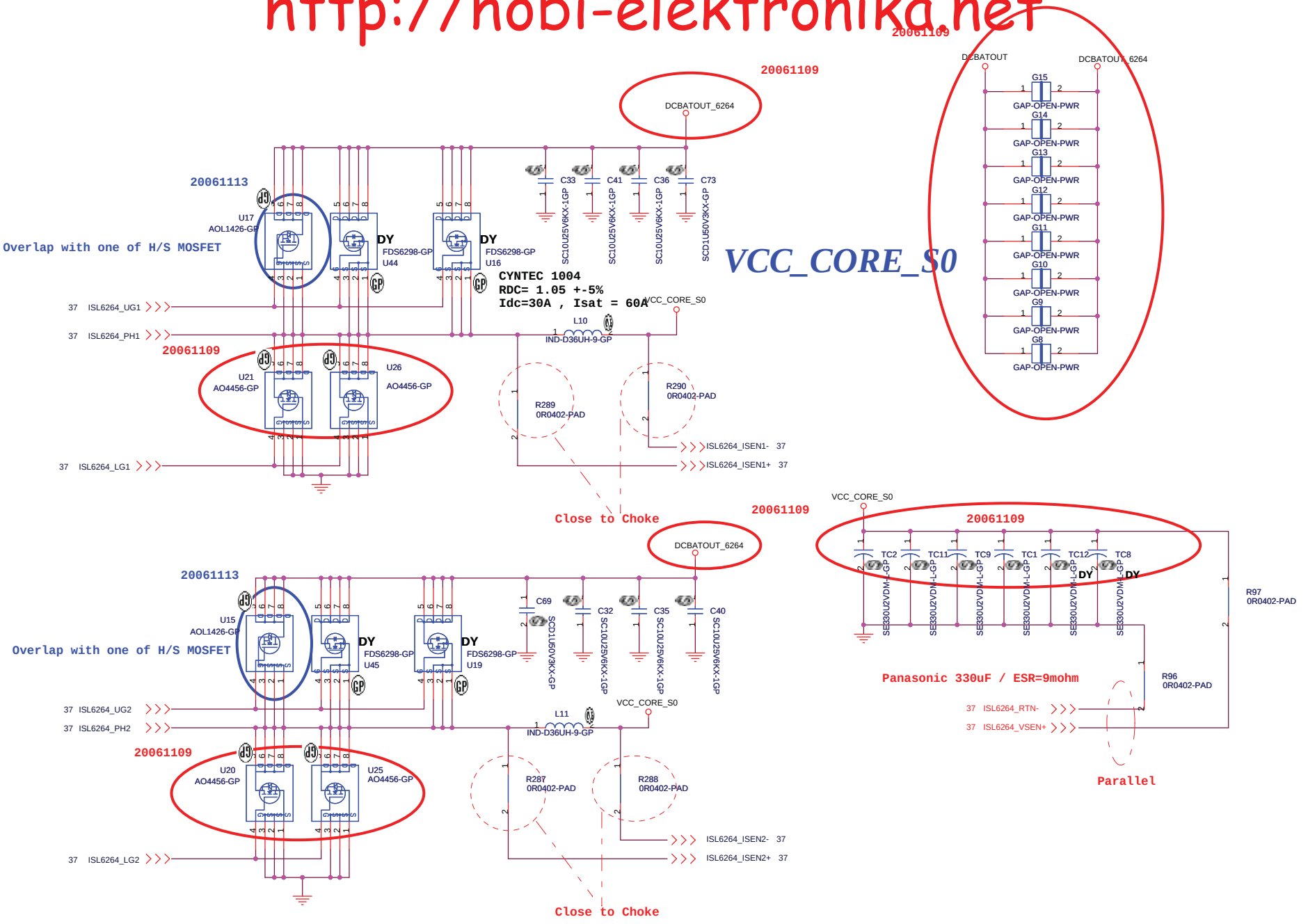
<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1

Size: A2 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 37 of 46



VCC_CORE_S0

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

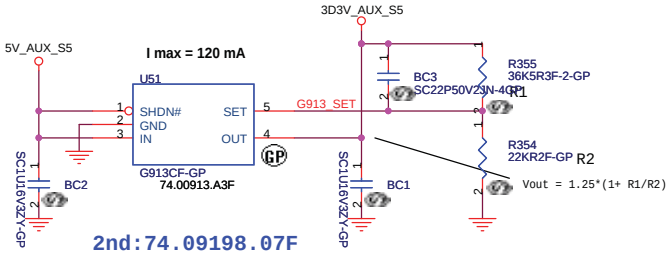
Title: CPU Vcore Power_2

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 38 of 46

Aux Power

3D3V_AUX_S5

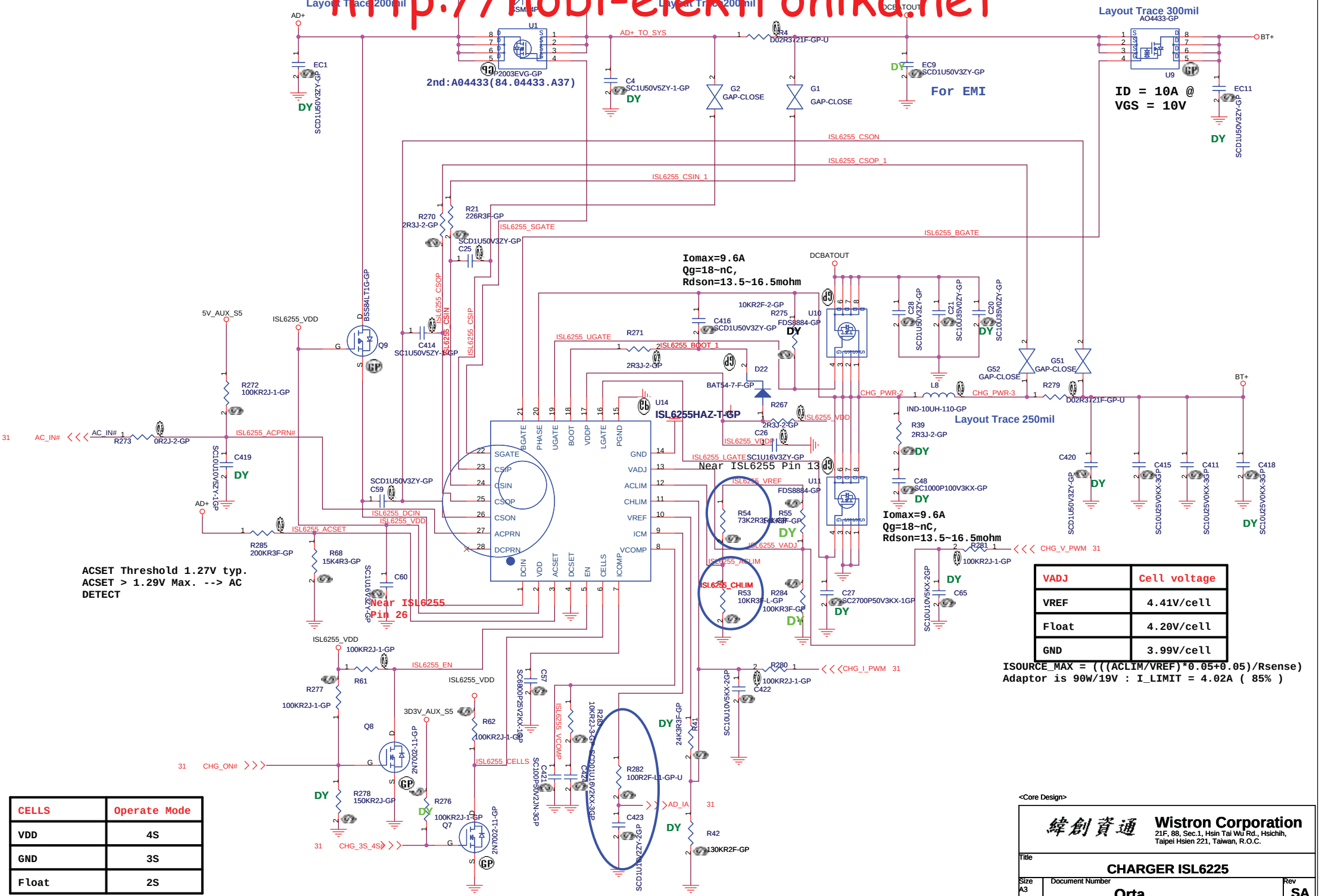


2nd:74.09198.07F
(RT9198-33PBG)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *3D3V_AUX*		
Size: A3	Document Number: **Orta**	Rev: **SA**
Date: Tuesday, December 12, 2006	Sheet 39 of 46	



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

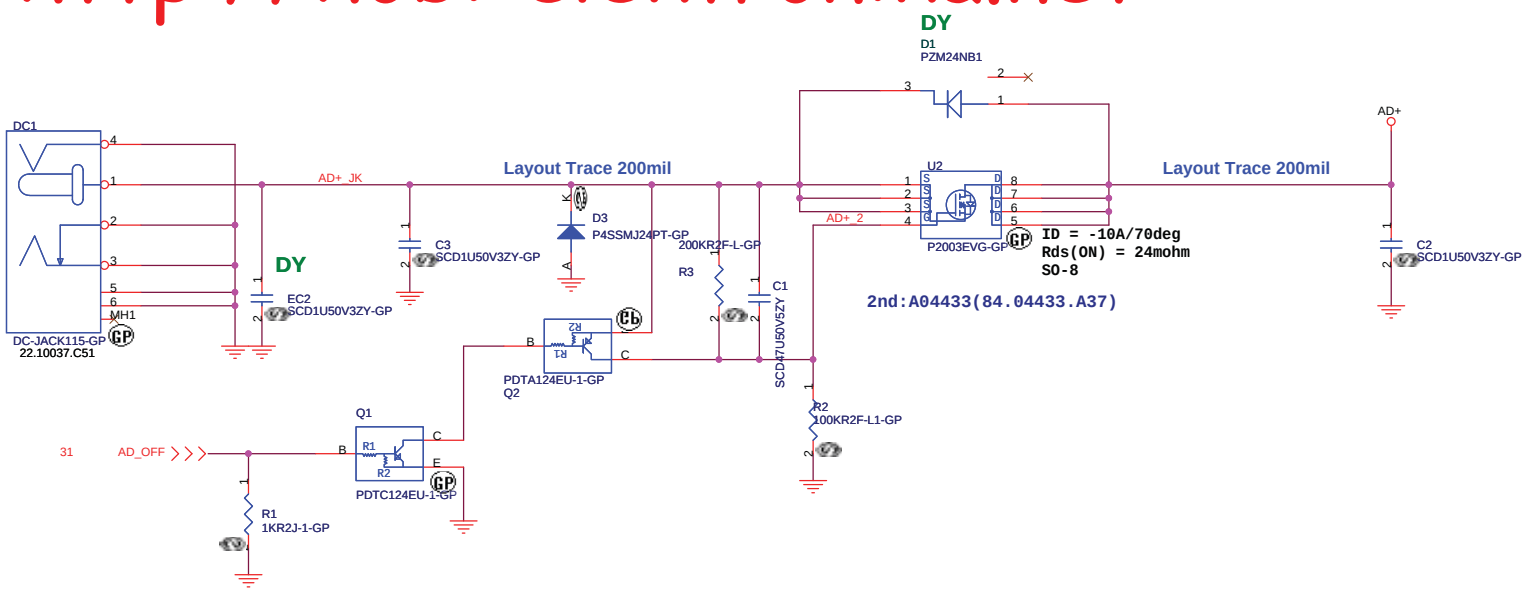
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

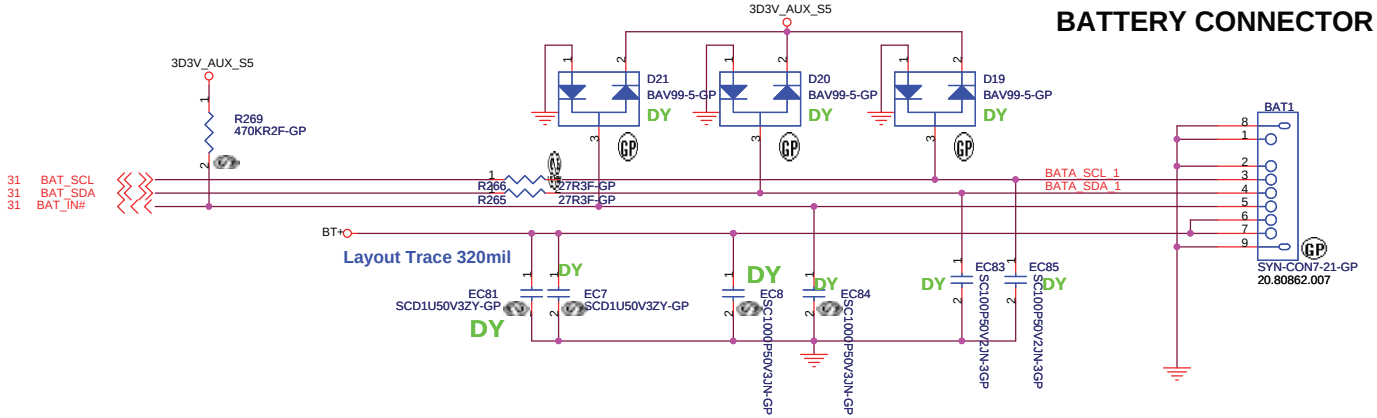
Title: CHARGER ISL6225

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 40 of 46



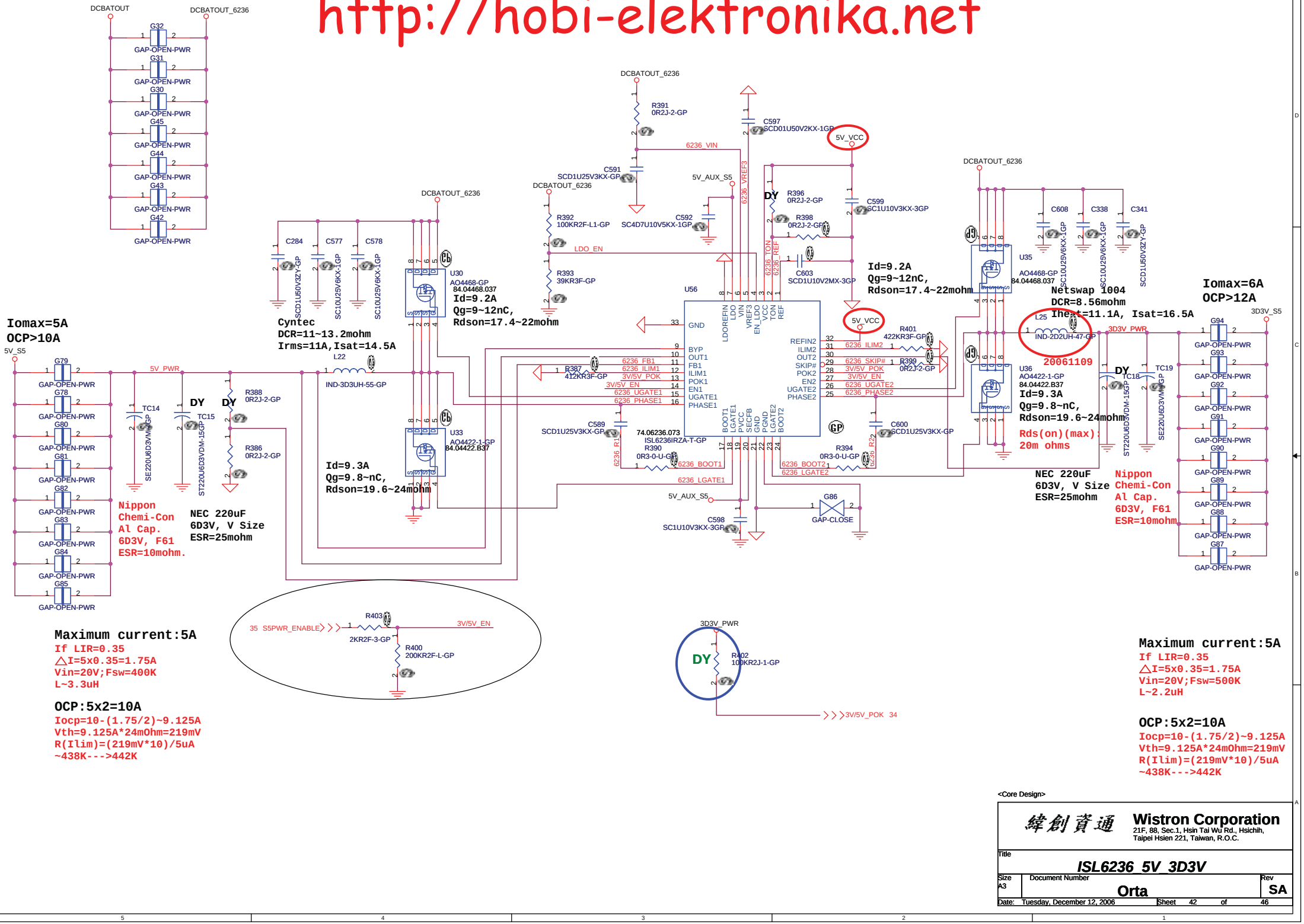
BATTERY CONNECTOR



<Variant Name>

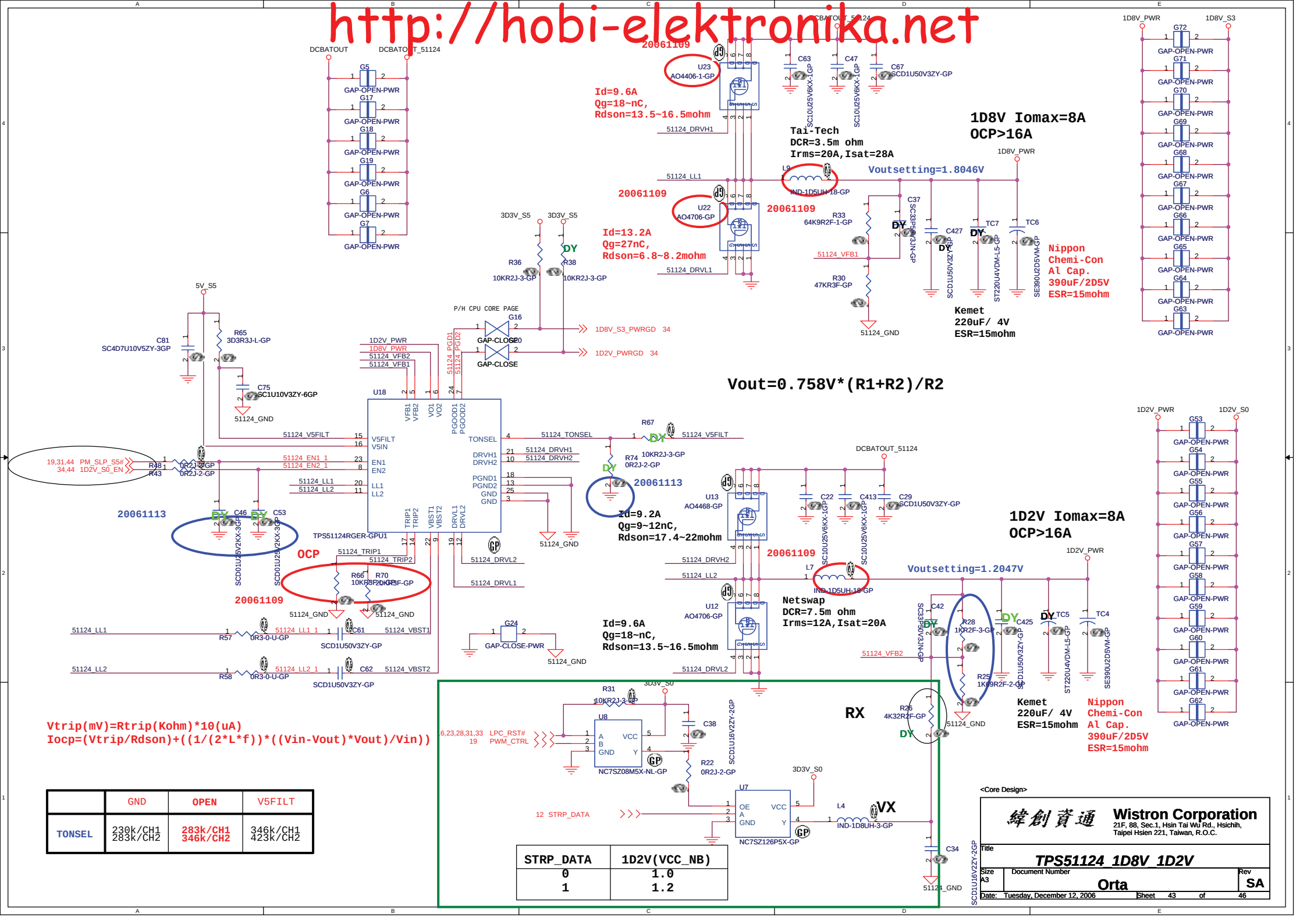
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number Orta	Rev SA
Date: Tuesday, December 12, 2006	Sheet 41 of 46	



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL6236_5V_3D3V
Size A3 / Document Number	Orta / Rev SA
Date: Tuesday, December 12, 2006	Sheet 42 of 46



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

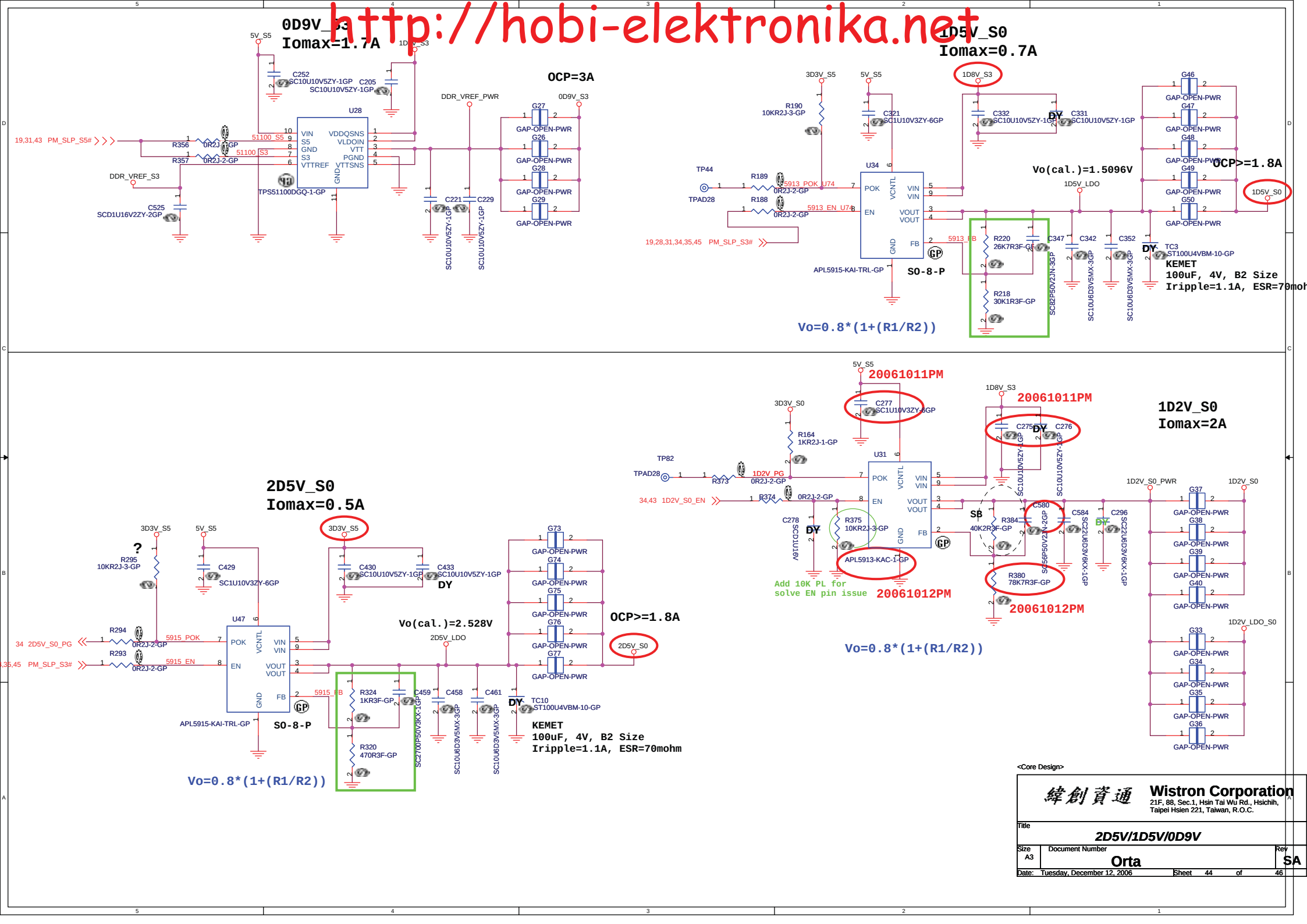
STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

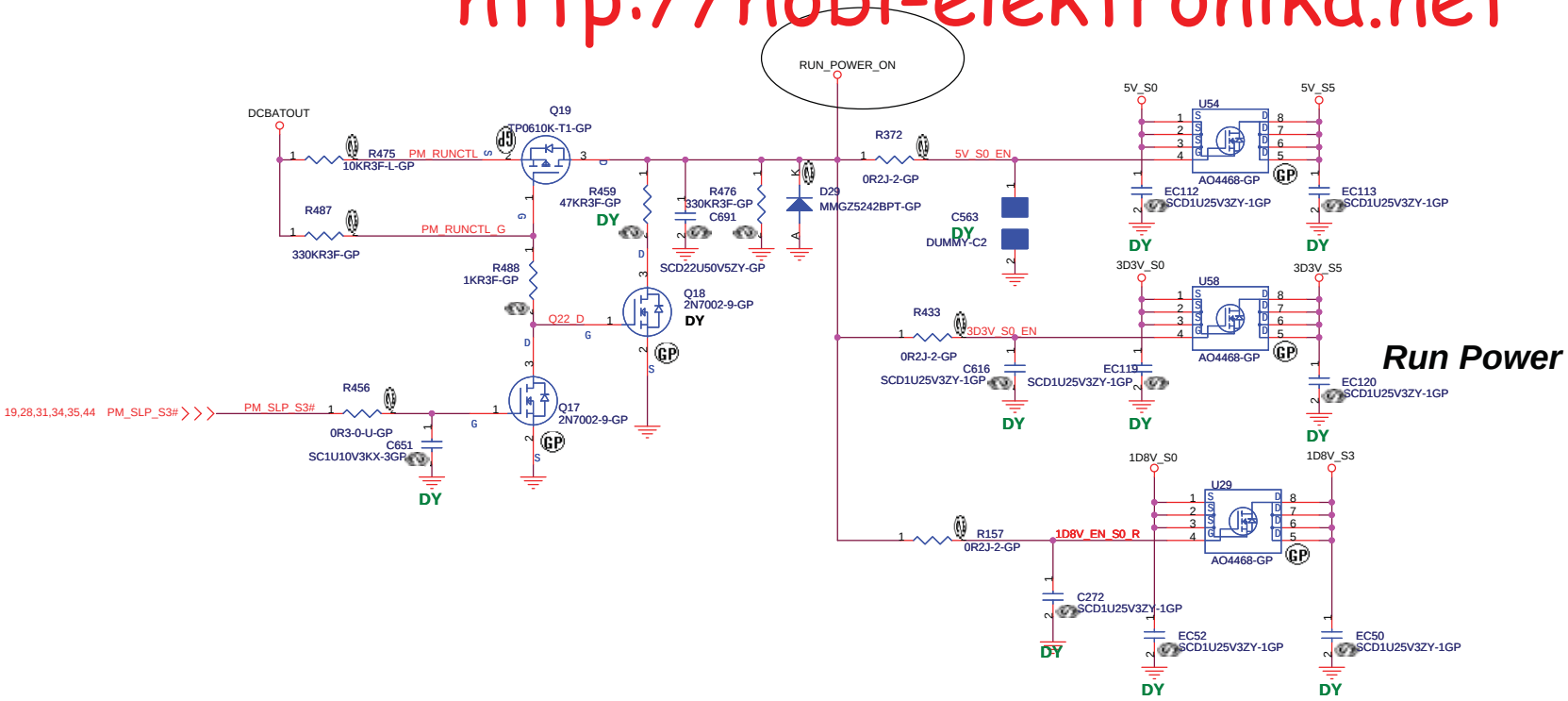
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D2V

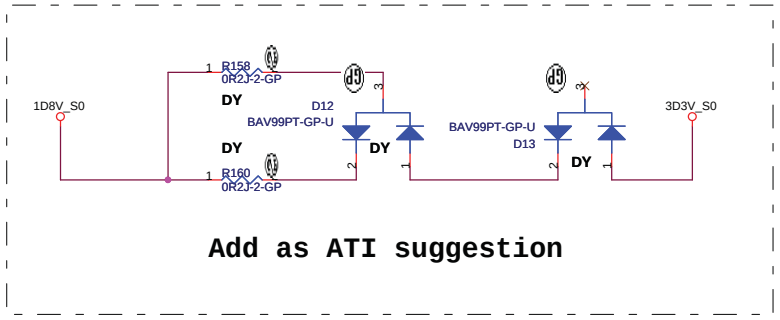
Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 43 of 46





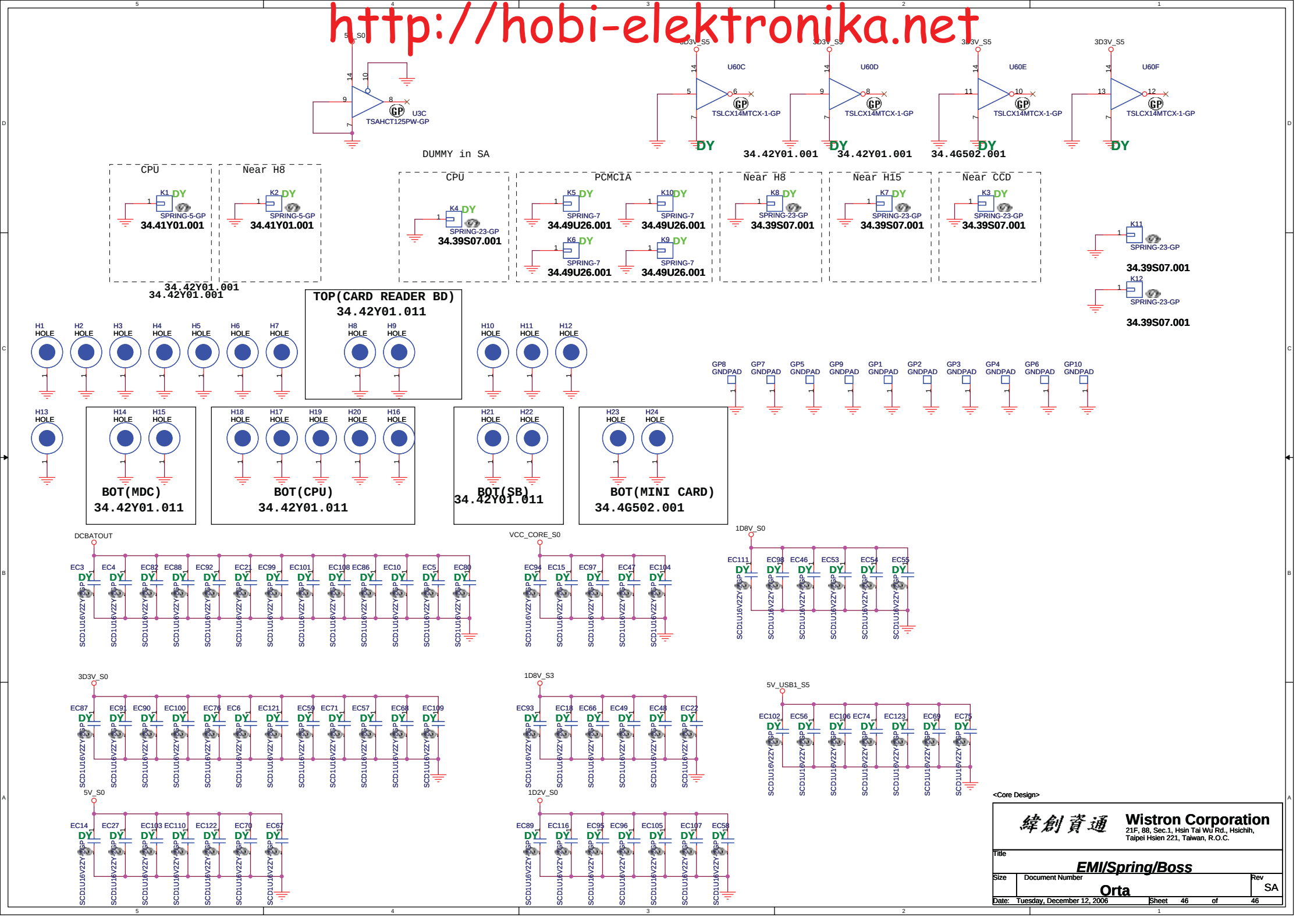
Run Power



Power On Logic

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWR CTL LOGIC / PWR PLANE		
Size: A3	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 45 of 46	



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***EMI/Spring/Boss***
Size / Document Number	**Orta**
Rev	SA
Date: Tuesday, December 12, 2006	Sheet 46 of 46